UNIVERSITY OF SWAZILAND

SUPPLEMENTARY EXAMINATION 2005

Title of paper: INTRODUCTION TO LOGIC

Course number: CS235

Time allowed: Three (3) hours

Instructions: Answer any five (5) of the seven (7) questions.

This examination paper should not be opened until permission has been granted by the invigilator.

Question 1

(a) Consider the equivalence:

$$\neg P \wedge \neg Q \wedge \neg R \equiv \neg(P \vee Q \vee R)$$

(i) Prove the correctness of the equivalence by truth table. [7]

(ii) State the dual of the equivalence. [3]

(b) Consider the proposition:

$$A \wedge (B \Rightarrow C) \Leftrightarrow A \vee B \wedge \neg C$$

(i) Prove by truth table that the proposition is contingent. [8]

(ii) How many models satisfy the proposition? [2]

Question 2

(a) State the *overlap* law of equivalence. [2]

(b) Prove the correctness of the overlap law using other laws of equivalence. [4]

(c) Simplify the following propositions using laws of equivalence:

(i) $A \wedge \neg((A \Rightarrow B) \vee C)$ [6]

(ii) $(A \vee \mathbf{T}) \wedge (A \vee B) \Leftrightarrow C \vee \neg(D \Rightarrow C)$ [8]

Question 3

Verify the following by natural deduction:

(a) C
$\underline{A \Leftrightarrow B \Rightarrow C}$
A

[6]

(b) $(A \vee C) \wedge (B \vee C)$
$\underline{\neg (C \vee D)}$
B

[6]

(c) $A \wedge B \Rightarrow \neg C$
$C \Leftrightarrow B \Rightarrow D$
$\underline{B \wedge C}$
$\neg A \wedge D$

[8]

Question 4

(a) Minimize the following Boolean function using a Karnaugh map:

$$f(a, b, c, d) = abc + \bar{a}.\bar{b}.\bar{d} + a\bar{b}cd + a\bar{b}.\bar{c}.\bar{d}$$

Assume that the following 2 are impossible inputs:

$$a\bar{b}c\bar{d}$$

$$\bar{a}.\bar{b}cd$$

[10]

(b) Draw a circuit that implements the minimized expression given in the answer to part (b). Use only NAND gates in the circuit.

[10]

Question 5

(a) Distinguish between *combinational* and *sequential* logic circuits.

[2]

(b) Draw a complete circuit diagram of an RS-latch, showing all logic gates contained in the device.

[6]

(c) Describe how RS-latches may be used to construct a JK-flip-flop.

[6]

(d) Describe how the values stored within a JK-flip-flop will vary in response to input from a clock.

[6]

Question 6

Design a logic circuit that will take input from a clock and produce output in the form of a repeating sequence of integers from 16 down to 1 as follows: 16, 15, 14, ..., 3, 2, 1, 16, 15, 14, ..., 3, 2, 1, 16, ...

The outputs of the circuit must be labelled S0, S1, S2, S3 and S4, each corresponding to one of the 5 binary digits of the output integer, starting from the least significant (or rightmost) digit, S0, and progressing to the most significant (or leftmost) digit , S4.

[20]

Question 7

(a) Copy the following predicates and circle each occurrence of a *bound* variable:

$$A(x) \wedge \exists x(B(y)) \wedge \forall x(C(x))$$

$$\forall w(\forall x(P(w, x) \wedge \exists y(\exists z(Q(x, y)))) \wedge R(w, x))$$

[6]

(b) Rewrite the following predicate such that <u>all</u> variables are *universally* quantified:

$$\neg\forall x(\exists y(P(x, y) \Rightarrow Q(x, y) \wedge \exists z(Q(y, z))))$$

[6]

(c) Give a model of the first predicate that is <u>also</u> a model of the second predicate:

$$\forall x(P(x) \wedge Q(x) \Rightarrow R(x))$$

$$\exists x(\neg P(x) \wedge \neg Q(x) \wedge \neg R(x))$$

[8]