UNIVERSITY OF SWAZILAND

FINAL EXAMINATION 2005

Title of paper: COMPUTER ORGANISATION II

Course number: CS341

Time allowed: Three (3) hours

Instructions: Answer any five (5) of the seven (7) questions.

This examination paper should not be opened until permission has been granted by the invigilator.

Question 1

(a) Describe in detail the timing of the events occurring over a clock cycle in the Mic-1 microarchitecture.

[12]

(b) Describe in detail the effects of the following lines of Mic-1 microcode:

(i) Main interpreter loop microinstruction:

```
Main1     PC = PC + 1; fetch; goto (MBR)
```

(ii) Microinstructions for implementing the POP instruction. (Note that the second line is intentionally blank):

```
pop1      MAR = SP = SP - 1; rd
pop2
pop3      TOS = MDR; goto Main1
```

[8]

Question 2

(a) Explain why a 3-bus microarchitecture permits a shorter execution path length than a 2-bus microarchitecture.

[4]

(b) Explain how an *instruction fetch unit* can help to reduce the load on the ALU.

[4]

(c) Give an overview of the seven-stage pipeline of the Mic-4 microarchitecture.

[12]

Question 3

(a) Define the RAW, WAR and WAW inter-instruction dependencies. Give an example of each.

[6]

(b) Give an overview of the *direct-mapped* and *set-associative* caching strategies. How are *cache hits* detected in each strategy?

[14]

Question 4

Give an overview of the *instruction set architecture level* of the Pentium II processor.

[20]

Question 5

(a) Describe the *immediate*, *direct* and *indirect* addressing modes.

[5]

(b) Determine the smallest number of bits required to encode instructions for an instruction set architecture with 5 instructions, each taking 1 register operand and 1 address operand. There are 13 registers and 10,000 bytes of addressable memory.

[6]

(c) Design an instruction set format for an architecture with a 21-bit instruction word. Each register operand must be encoded in 6 bits, and each address operand in 10 bits. There are 3 kinds of instructions:

(i) 5 instructions take 1 register operand and 1 address operand.
(ii) 2 instructions take 3 register operands.
(iii) 50 instructions take 1 address operand.

[9]

Question 6

(a) Consider the fragment of a Pentium assembly language program. What value will be found in the memory location labelled X just after the SUB instruction has been executed? Explain.

```
SEGMENT .text
     mov  ch, 0
     mov  cl, [Powers + 2]
     add  [X], cx
     mov  cl, [Powers + 3]
     sub  [X], cx
     ...

SEGMENT .data
Powers    DB 1, 2, 4, 8, 16
X         DW 500
```

[4]

(b) Write a Pentium assembly language program that inputs 100 characters from the keyboard, and finally displays the character having the greatest ASCII code out of all those input.

[6]

(c) Write a Pentium assembly language program that inputs 2 characters from the keyboard and then displays all characters in the ASCII series between the lesser input and the greater input. For example, if 'k' and then 'p' were input, 'klmnop' must be displayed, but if '9' and then '3' were input, '3456789' must be displayed.

[10]

Question 6

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[10]

Question 7

(a) Define the following processor-interconnection topologies: *star*, *tree*, *ring*, *grid* and *torus*.

[10]

(b) Give the *dimensionality* and *diameter* of each of the following topologies:

(i) Ring of 20 nodes.

(ii) 5-by-4 grid.

(iii) 5-by-4 torus.

[6]

(c) Describe the *dimensional routing* algorithm for grids.

[4]