UNIVERSITY OF SWAZILAND

SUPPLEMENTARY EXAMINATION 2005

Title of paper: COMPUTER ORGANISATION II

Course number: CS341

Time allowed: Three (3) hours

Instructions: Answer any five (5) of the seven (7) questions.

This examination paper should not be opened until permission has been granted by the invigilator.

Question 1

(a) Describe in detail the 4 memory control registers of the Mic-1 microarchitecture, and in particular, their role in mediating transfers between the CPU and main memory.

[8]

(b) Describe in detail the effects of the following lines of Mic-1 microcode:

(i) Main interpreter loop microinstruction:

```
Main1     PC = PC + 1; fetch; goto (MBR)
```

(ii) Microinstructions for implementing the IADD instruction:

```
iadd1     MAR = SP = SP - 1; rd
iadd2     H = TOS
iadd3     MDR = TOS = MDR -H; wr; goto Main1
```

[12]

Question 2

(a) What is a *shift register*? How may it be employed in the design of an instruction fetch unit?

[4]

(b) (i) Give an overview of the four-stage pipeline of the Mic-3 microarchitecture.

[7]

(ii) The following microcode is used by the un-pipelined Mic-2 microarchitecture to implement the ISTORE instruction. (Note that the fourth line is intentionally blank):

```
istore1         MAR = LV + MBR1U
istore2         MDR = TOS; wr
istore3         MAR = SP = SP - 1; rd
istore4
istore5         TOS = MDR; goto (MBR1)
```

Give the *microsteps* that are performed in each cycle by Mic-3 while executing the above microcode. How many cycles are taken to execute all 5 microinstructions?

[9]

Question 3

(a) Describe the *write-through*, *write-back* and *write-allocation* methods of dealing with cache writes.

[6]

(b) Describe a branch prediction method based on 2-bit history tables.

[8]

(c) A two-level cache experiences a 70% hit rate at level 1. Requests that miss level 1 experience a 50% hit rate at level 2. What is the average access time, given that:

- Time to request and fetch from level 1 cache is 5 ns.
- Additional time to request and fetch from level 2 cache is 10 ns.
- Additional time to request and fetch from main memory is 100 ns.

[6]

Question 4

An *instruction set architecture* (ISA) comprises information that a programmer needs to know about in order to program in machine language. Give an overview of the kinds of information that need to be specified when describing any ISA, under the following headings:

(a) Privilege modes.
(b) Memory model.
(c) Registers.
(d) Instructions.

[20]

Question 5

(a) Describe the numeric data types supported by the Pentium II instruction set architecture.

[4]

(b) Determine the smallest number of bits required to encode instructions for an instruction set architecture with 64 instructions, each taking 2 register operands and 1 address operand. There are 8 registers and 2,048 bytes of addressable memory.

[5]

(c) Design an instruction set format for an architecture with a 24-bit instruction word. Each operand, whether a register or an address, must be encoded in 8 bits. There are 3 kinds of instructions:

(i) 32 instructions take no operands.
(ii) 8 instructions take 1 operand.
(iii) 200 instructions take 2 operands.

[4]

(d) Design an instruction set format for an architecture with a 32-bit instruction word. Each register operand must be encoded in 3 bits, and each address operand in 9 bits. There are 2 kinds of instructions:

(i) 3 instructions take 1 register operand and 3 address operands.
(ii) 200 instructions take 4 register operands.

[7]

Question 6

(a) Consider the fragment of a Pentium assembly language program. What value will be found in the BX register just after the DEC instruction has been executed? Explain.

```
SEGMENT .text
     mov  bl, [X]
     inc  bl
     mov  bh, [X + 1]
     dec  bh
     ...

SEGMENT .data
X    DB 1, 2
```

[4]

(b) Write a Pentium assembly language program that repeatedly inputs characters from the keyboard, until a non-alphabetic character is typed, whereupon it should terminate immediately. As each character is typed, it should display one of 2 messages: 'Upper' if the character is an upper-case letter, or 'Lower' if it is a lower-case letter.

[8]

(c) Write a Pentium assembly language program that repeatedly inputs characters from the keyboard, until the letter 'x' is typed thrice consecutively, whereupon it should terminate immediately.

[8]

Question 7

(a) Explain how the speedup of a program, running on an N-processor parallel computer, may be calculated.

[5]

(b) Explain why *linear speedup* of programs is not normally achievable.

[7]

(c) Distinguish between the following pairs of concepts:

(i) Degree and diameter of a topology.

(ii) Shared- and distributed-memory systems.

(iii) Circuit switching and store-and-forward packet switching.

(iv) Source routing and distributed routing.

[8]