University of Swaziland

Faculty of Science
Department of Computer Science

Final Examination, 2006/07

Title of Paper: Computer Organisation I

Course Number: CS241

Time Allowed: Three (3) hours

Instruction: Answer all questions. Questions carry equal marks.

You are reminded that in assessing your work, account will be taken of the accuracy of the material, of the language used and the general quality of expression, together with the layout and presentation of your answer. Remember full answers will usually *define, explain and exemplify.*

Special Requirement:

Calculators are prohibited.

This examination paper should not be opened until permission has been granted by the invigilator.

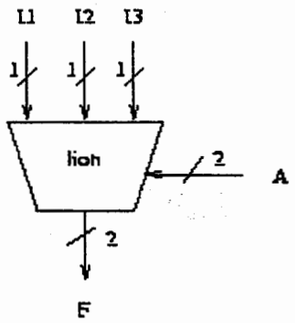
Question 1.
Referring to figure 1,
a) Give the micro-code that is executed when the MIR of Tanenbaum's Mic1 subset of JVM contains:

540390211_{16}

b) Translate the following micro-code into the bits of the MIR and write the answer in octal.

MAR = SP = SP - 1; read

Question 2.
The following defines an arithmetic and logical unit:



A_1	A_2	F
0	0	$I_1 + (I_2$ OR $I_3)$
0	1	I_2 AND I_3 OR I_2
1	0	$I_3 + I_2 - I_1$
1	1	$I_1 + I_2 + I_3$
		+ and - are arithmetic

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a) What is the output when:

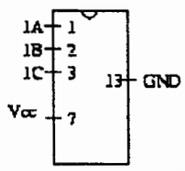
	I_1	I_2	I_3	A_1	A_2
i)	1	0	1	1	0
ii)	1	0	1	0	0
iii)	0	1	1	0	1

b) When:
$I_1 = I_2 = I_3 = A_1 = A_2 = 1$
what happens?

Question 3.
a) Differentiate between the environment variables CLASSPATH and PATH.

b) What is an applet?

c) From this diagram alone, describe the operation of the chip.



d) What is anonymous FTP?

e)Describe at least two methods that manufacturers use to identify which way round to put connectors onto their ribbon cables.

Question 4.

a) Express -20_{10} in binary.

b) Convert 2469_{10} into hexadecimal.

c) Convert 129_{16} to octal.

d) In what circumstances would you choose Java and not JVM to write a program?

Question 5.

a) Show how the AND logic function can be implemented using transistors. Explain all the components.

b) How do you implement a two input OR gate using NAND gates only? (How do you know it works?)

Addr(9)	J (3)			ALU (8)								C (9)									M (3)			B (4)
				shifter		ALU proper																		
address in the control store of next micro-instruction to be obeyed	JMPC	JAMN	JAMZ	SLL8	SRA1	F_0	F_1	enable H reg	enable B bus	invert H reg	increment output	H	OPC	TOS	CPP	LV	SP	PC	MDR	MAR	write	read	fetch	one only of: 0 = MDR 1 = PC 2 = MBR 3 = MBRU 4 = SP 5 = LV 6 = CPP 7 = TOS 8 = OPC 9 – 15 undefined

what appears on o/p of ALU	F_0	F_1	enable I/P from H reg	enable I/P from B bus	invert I/P from H reg	force carry to LSbit of O/P
Hreg	0	1	1	0	0	0
Bbus	0	1	0	1	0	0
not(H)	0	1	1	0	1	0
not(Bbus)	1	0	1	1	0	0
H + Bbus	1	1	1	1	0	0
H + Bbus + 1	1	1	1	1	0	1
H + 1	1	1	1	0	0	1
Bbus + 1	1	1	0	1	0	1
Bbus – H	1	1	1	1	1	1
Bbus – 1	1	1	0	1	1	0
-H	1	1	1	0	1	1
H and Bbus	0	0	1	1	0	0
H or Bbus	0	1	1	1	0	0
0	0	1	0	0	0	0
1	0	1	0	0	0	1
-1	0	1	0	0	1	0

F_0	F_1	ALU function
0	0	Hreg and Bbus
0	1	Hreg or Bbus
1	0	not(Bbus)
1	1	Hreg + Bbus

Figure 1: A reminder of the tables introduced during the course, defining the MIC1.

End of examination paper.