University of Swaziland

Faculty of Science
Department of Computer Science

Final Examination, May 2008

Title of Paper: Computer Organisation I

Course Number: CS241

Time Allowed: Three (3) hours

Instruction: Answer at least five questions. Questions carry equal marks.

You are reminded that in assessing your work, account will be taken of the accuracy of the material, of the language used and the general quality of expression, together with the layout and presentation of your answer. Remember full answers will usually *define, explain and exemplify*. The use of a calculator is prohibited.

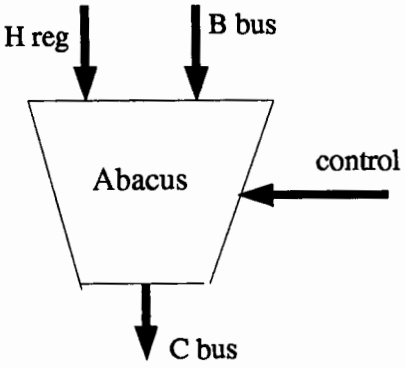
Special Requirement:

Calculators are prohibited.

This examination paper should not be opened until permission has been granted by the invigilator.

Question 1. [20]
The following is the definition of the Abacus ALU.

<control> ::= <enable H> <enable B> <function>



function	operation
00	H + B
01	H + B with carry
10	H & B
11	H + 1
+ is arithmetic	

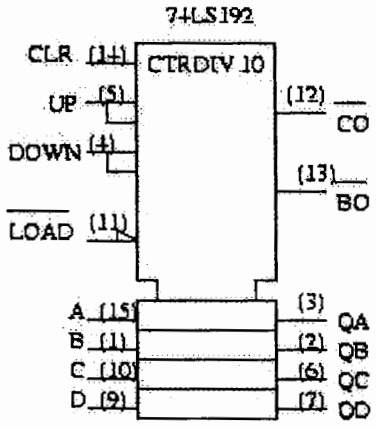
What appears on the C bus with H reg being 5_{10} and the B bus having 15_{10} when control is
a) 0XE
b) 013
c) 15_{10}
d) 8_{16}

What information is not given in the definition?

Question 2. [20]
a) What happens when the MIR of Tanenbaum's machine contains:
042015320307_8

b) Translate this microcode into the MIR format, and express it in base sixteen:
MAR = SP = SP - 1; RD

Question 3. [20]
Draw a possible pin-out diagram from this logic symbol:



Question 4. [20]
Draw the transistor circuit diagram for a 3-input OR gate.
Derive from first principles its output.

Question 5. [20]
Explain *folding* in PicoJava. Give the reason(s) for its being included in the design of the VM.

Question 6. [20]
Explain these terms:
a) *present and stable*
b) *bus*
c) USB
d) little endian
e) UART

A reminder of the tables introduced during the course, defining the MIC1.

Addr(9)	J (3)			ALU (8)								C (9)									M (3)			B (4)
				shifter		ALU proper																		
address in the control store of next micro-instruction to be obeyed	JMPC	JAMN	JAMZ	SLL8	SRA1	F_0	F_1	enable H reg	enable B bus	invert H reg	increment output	H	OPC	TOS	CPP	LV	SP	PC	MDR	MAR	write	read	fetch	one only of: 0 = MDR 1 = PC 2 = MBR 3 = MBRU 4 = SP 5 = LV 6 = CPP 7 = TOS 8 = OPC 9 - 15 undefined

F_0	F_1	ALU function
0	0	Hreg and Bbus
0	1	Hreg or Bbus
1	0	not(Bbus)
1	1	Hreg + Bbus

what appears on o/p of ALU	F_0	F_1	enable I/P from H reg	enable I/P from B bus	invert I/P from H reg	force carry to LSbit of O/P
Hreg	0	1	1	0	0	0
Bbus	0	1	0	1	0	0
not(H)	0	1	1	0	1	0
not(Bbus)	1	0	1	1	0	0
H + Bbus	1	1	1	1	0	0
H + Bbus + 1	1	1	1	1	0	1
H + 1	1	1	1	0	0	1
Bbus + 1	1	1	0	1	0	1
Bbus - H	1	1	1	1	1	1
Bbus - 1	1	1	0	1	1	0
- H	1	1	1	0	1	1
H and Bbus	0	0	1	1	0	0
H or Bbus	0	1	1	1	0	0
0	0	1	0	0	0	0
1	0	1	0	0	0	1
-1	0	1	0	0	1	0

End of examination paper