University of Swaziland

Faculty of Science
Department of Computer Science

Supplementary Examination, July 2008

Title of Paper: Computer Organisation I

Course Number: CS241

Time Allowed: Three (3) hours

Instruction: Answer five questions. Questions carry equal marks.

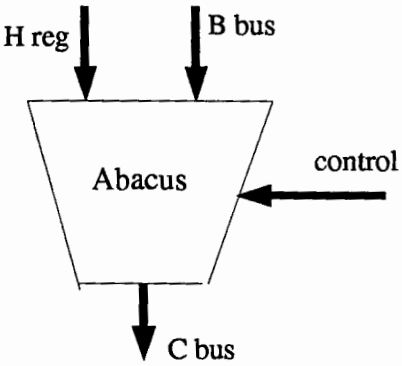
You are reminded that in assessing your work, account will be taken of the accuracy of the material, of the language used and the general quality of expression, together with the layout and presentation of your answer. Remember full answers will usually *define, explain and exemplify*. The use of a calculator is prohibited.

Special Requirement:

Calculators are prohibited.

This examination paper should not be opened until permission has been granted by the invigilator.

Question 1. [20]
The following is the definition of the Abacus ALU.



control	operation
011	H OR B
001	H + B
110	H + B + 2
010	H & B
111	H + B + 3
000	H - B
+ - are arithmetic	

What appears on the C bus when the values of the H reg are as in the *temp* column and the register being accessed on the B bus having the values in the *time* column of the following table:

	temp	time	control
a)	20_{10}	F_{16}	0
b)	$7F_{16}$	FF_{16}	2_{10}
c)	444_8	9_{10}	110_2
d)	10101_2	7_8	011_2

What information is not given in the definition?

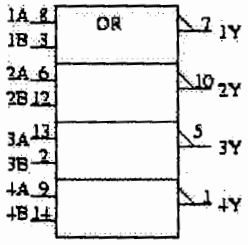
Question 2. [20]
a) What happens when the MIR of Tanenbaum's machine contains:

000 000 000 000 001 011 001 100 000 000 010 001_2

b) Translate this microcode into the MIR format, and express it in base eight:

MAR = CPP + H; rd

Question 3. [20]
Draw a possible pin-out diagram from this logic symbol:



Question 4. [20]
Draw the transistor circuit diagram for a 4-input OR gate.
Derive from first principles its output.

Question 5. [20]
Explain, with a diagram, the pipline of the 486 and Pentium I.

Contrast it with the equivalent construct of the Pentium II.

Question 6. [20]
Explain these terms:
a) strongly typed
b) ISA
c) flash prom
d) big endian
e) pnp junction

A reminder of the tables introduced during the course, defining the MIC1.

Addr(9)	J (3)			ALU (8)								C (9)								M (3)			B (4)
				shifter		ALU proper																	
address in	JMPC	JAMN	JAMZ	SLL8	SRA1	F_0	F_1	enable	enable	invert	increment	H	OPC	TOS	CPP	LV	SP	PC	MDR	MAR	write	read	fetch	one only of:
the control								H reg	B bus	H reg	output													0 = MDR
store of next																								1 = PC
micro-																								2 = MBR
instruction to																								3 = MBRU
be obeyed																								4 = SP
																								5 = LV
																								6 = CPP
									F_0	F_1	ALU function													7 = TOS
																								8 = OPC
									0	0	Hreg and Bbus													9 – 15 undefined
									0	1	Hreg or Bbus													
what appears	F_0	F_1	enable I/P	enable I/P	invert I/P	force carry t			1	0	not(Bbus)													
on o/p of ALU			from H reg	from B bus	from H reg	LSbit of O/P			1	1	Hreg + Bbus													
Hreg	0	1	1	0	0	0																		
Bbus	0	1	0	1	0	0																		
not(H)	0	1	1	0	1	0																		
not(Bbus)	1	0	1	1	0	0																		
H + Bbus	1	1	1	1	0	0																		
H + Bbus + 1	1	1	1	1	0	1																		
H + 1	1	1	1	0	0	1																		
Bbus + 1	1	1	0	1	0	1																		
Bbus – H	1	1	1	1	1	1																		
Bbus – 1	1	1	0	1	1	0																		
- H	1	1	1	0	1	1																		
H and Bbus	0	0	1	1	0	0																		
H or Bbus	0	1	1	1	0	0																		
0	0	1	0	0	0	0																		
1	0	1	0	0	0	1																		
-1	0	1	0	0	1	0																		

End of examination paper