UNIVERSITY OF SWAZILAND

Faculty of Science

Department of Computer Science

Supplementary Examination, July 2010

Title of paper: **COMPUTER ORGANISATION - I**

Course numbers: **CS241**

Time allowed: 3 hours

Instructions: • Answer any 5 out of the 6 questions. Each question carries 20 marks.

• **The use of electronic calculators is forbidden.**

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Question 1

Write short notes on any 3 of the following topics:

a) Fetch-decode-execute cycle
b) Word size
c) Superscalar architecture
d) Cache memory
e) Bus arbitration [20]

Question 2

a)

i. Write the integer -13 in twos complement notation using 5 bits. [2]

ii. Write the 12 bit integer 010111100001_2 in hexadecimal and octal notations. [2]

iii. On a byte addressed machine, the integer 123456_{16} is stored in main memory starting at address 500. At what addresses are the constituent bytes stored? In addition, what values are stored at each address, assuming that big endian byte ordering is used? [4]

b)

i. In the IEEE single-precision floating point formats, how many bits are allocated to each field? [2]

ii. Convert $3FC00000_{16}$ from IEEE single-precision floating point format into decimal notation (real number with decimal point). [4]

iii. Explain the following terms in relation to floating point:

- Overflow and underflow errors
- Excess notation
- Degenerate coding [6]

Question 3

a) Draw a circuit showing 2 transistors connected together to form a NOR gate. [3]

b) Draw the following logic circuits:

i. 4-bit multiplexer. [6]

ii. A circuit that inputs a 4-bit non-negative integer (*N*) and outputs *2*(N+1)*. The circuit must include a left shifter and some 1-bit adders. [11]

Question 4

a)

i. Draw the D-flip-flop's action table. [4]

ii. Draw a logic circuit of a clocked D-flip-flop that changes state on the rising edge of the clock. [7]

b) Briefly describe the difference between the following pairs of memory technologies:

i. RAM and ROM.
ii. SRAM and DRAM.
iii. FPM DRAM and EDO DRAM.
iv. PROM and EPROM.
v. EEPROM and flash memory. [9]

Question 5

a) Explain the purpose of the following main-memory areas of the IJVM virtual machine:

i. Operand stack
ii. Local variable frame
iii. Method area [6]

b) How are the Mic-1's registers MAR, MDR, PC and MBR used to assist the CPU to communicate with main memory? [4]

c) Comment in detail on Mic-1's implementation (given below) of IJVM's ISTORE instruction: [10]

```
istore1         H = LV
istore2         MAR = MBRU + H
istore3         MDR = TOS; wr
istore4         SP = MAR = SP - 1; rd
istore5         PC = PC + 1; fetch
istore6         TOS = MDR; goto Main1
```

Question 6

a) Translate the following Java code into IJVM assembly language: [13]

```
if (b < 1)
  b = 1;
a = a + a - b - b;
```

b) Translate your assembly language program from question a) into IJVM machine code (refer to the table of IJVM opcodes below). [7]

Hex	Mnemonic	Meaning
0x10	BIPUSH *byte*	Push byte onto stack
0x59	DUP	Copy top word on stack and push onto stack
0xA7	GOTO *offset*	Unconditional branch
0x60	IADD	Pop two words from stack; push their sum
0x7E	IAND	Pop two words from stack; push Boolean AND
0x99	IFEQ *offset*	Pop word from stack and branch if it is zero
0x9B	IFLT *offset*	Pop word from stack and branch if it is less than zero
0x9F	IF_ICMPEQ *offset*	Pop two words from stack; branch if equal
0x84	IINC *varnum const*	Add a constant to a local variable
0x15	ILOAD *varnum*	Push local variable onto stack
0xB6	INVOKEVIRTUAL *disp*	Invoke a method
0x80	IOR	Pop two words from stack; push Boolean OR
0xAC	IRETURN	Return from method with integer value
0x36	ISTORE *varnum*	Pop word from stack and store in local variable
0x64	ISUB	Pop two words from stack; push their difference
0x13	LDC_W *index*	Push constant from constant pool onto stack
0x00	NOP	Do nothing
0x57	POP	Delete word on top of stack
0x5F	SWAP	Swap the two top words on the stack
0xC4	WIDE	Prefix instruction; next instruction has a 16-bit index