UNIVERSITY OF SWAZILAND

Faculty of Science
Department of Computer Science

Main Examination, May 2011

Title of paper: **COMPUTER ORGANISATION I**

Course numbers: **CS241**

Time allowed: 3 hours

Instructions: Answer any 4 out of the 5 questions. Each question carries 25 marks.

<u>THIS EXAMINATION PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GRANTED BY THE INVIGILATOR</u>

Question 1

a) Draw a diagram showing a NOR gate constructed using 2 transistors. [4]

b) A chip has 5 input and 32 output pins. The output pins are numbered from 0 to 31. Upon testing, the chip is always seen to output a 1 on pin number X, where X is the input integer; meanwhile 0 is output on all other pins.

   i. What is the full name of this device? [1]

   ii. What type of logic gates are required to build this device? State how many of each type are needed. [2]

   iii. In addition to the 37 pins for data input and output, there are 2 other pins in this chip. Name both pins and state their purpose. [2]

c) Draw a circuit diagram of a 3-bit comparator. [3]

d) Draw a circuit diagram of a 4-input multiplexer. [5]

e) Draw a circuit diagram of a subtraction circuit that inputs two 4-bit integers, X and Y, and outputs their difference, i.e. X-Y. Draw the adders in your diagram in the form of chips. [8]

Question 2

a) Suppose that the following byte values (shown in hexadecimal) are found in 4 consecutive memory locations starting at address 256:

   80 40 02 01

   i. What is the 2-byte value at address 258, assuming big-endian representation?

   ii. What is the 4-byte value at address 256, assuming little-endian representation?

   [2]

b) Suppose that it has become necessary to write some data, and that the choice has to be made between using either RAM or hard disk drive for storage. What further information is needed in order to make an appropriate choice? Give reasons.   [7]

c) Distinguish between each of the following pairs:
   i. Bus master and slave.

   ii. Synchronous and asynchronous buses.   [4]

d) Define each of the following, and explain how each one can improve computer performance:
   i. DMA

   ii. Cache

   iii. Instruction pipeline

   iv. Superscalar architecture   [12]

Question 3

a) State the full name and purpose of the following pins in memory chips: CS, OE, WE and RAS. [4]

b) An FPM-type memory chip has 7 pins for address input and 2 pins for data input/output.
   i. Draw the pin diagram of the chip including strobe lines. [3]

   ii. Work out the memory capacity of this chip. [2]

c) Draw a circuit diagram of a 2 x 2 memory comprised of 4 D-type flip flops. It is required to have the following inputs and outputs:
   - CS, RD and OE control inputs.
   - 2 data output lines, D_0 and D_1; and 2 data input lines, N_0 and N_1.
   - 1-bit address line, A. [16]

Question 4

a) Explain in detail the main steps comprising the fetch-decode-execute cycle. [8]

b) Briefly describe each of the 4 subcycles of the data path cycle. [4]

c) What is the purpose of a microcode assembler? [1]

d) The Mic-1 CPU has 2 memory ports. Distinguish between them. In addition, describe how the 4 memory control registers are used to operate these ports. [6]

e) The following Mic-1 microinstruction will lead to the propagation of several control signals. For each control signal, precisely state where it will be directed, and what effects it will cause upon arrival.
   MAR = SP = SP – 1; rd [6]

Question 5

Write four Mic-1 microprograms to carry out the following tasks:

a) Swap the SP and MAR registers. [3]

b) Add 1 to the word at memory address zero. [7]

c) Check whether H register is zero. If so, write 1 to H, otherwise write zero to H. [7]

d) Add together 3 words: one is found in the H register; another is in the OPC register; the third is in main memory, and its address is given in the SP register. Their sum must be stored in the H register. [8]

*** END OF PAPER ***

Mic-1 Data Sheet – List of ALU Functions

$$A, \ B, \ \bar{A}, \ \bar{B},$$
$$A+B, \ A+B+1, \ A+1, \ B+1,$$
$$B-A, \ B-1, \ -A,$$
$$A \text{ AND } B, \ A \text{ OR } B,$$
$$0, \ 1, \ -1$$

(The ALU's left and right inputs are denoted A and B, respectively.)