88

UNIVERSITY OF SWAZILAND

Faculty of Science

Department of Computer Science

Supplementary Examination, July 2011

Title of paper: **COMPUTER ORGANISATION - II**

Course numbers: **CS341**

Time allowed: 3 hours

Instructions: Answer any 5 out of the 6 questions. Each question carries 20 marks.

THIS EXAMINATION PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GRANTED BY THE INVIGILATOR

Question 1

(a) Write microinstruction code words for Mic-1's implementation of the IJVM IF_ICMPEQ instruction:

```
if_icmpeq1      MAR = SP = SP - 1; rd
if_icmpeq2      MAR = SP = SP - 1
if_icmpeq3      H = MDR; rd
if_icmpeq4      OPC = TOS
if_icmpeq5      TOS = MDR
if_icmpeq6      Z = OPC - H; if (Z) goto T; else goto F
```

Assume that the microinstructions of IF_ICMPEQ are at successive addresses in the control store, and that the addresses of the following microinstructions are:

- 0x01: Main1
- 0xFF: F [9]

(b) Determine whether or not the following Mic-1 microinstructions are valid (consider each line independently of the others). Explain the errors found in the invalid microinstructions.

1. TOS = SP
2. H = H + H
3. MBR = 1
4. H = TOS; MAR = MDR
5. rd; wr
6. if (N) goto Main1; else goto Main1 [6]

(c) Assuming that the current microinstruction in Mic-1 is a conditional branch, describe the sequence of steps by which the next microinstruction's address is determined. [5]

Question 2

(a) Describe the characteristics of a *shift register* and explain its purpose within the instruction fetch unit. [3]

(b) How many clock cycles does Mic-3 take to execute IJVM's ISTORE instruction (given below)? Clearly show the microsteps executed in each clock cycle.

```
istore1         MAR = LV + MBR1U
istore2         MDR = TOS; wr
istore3         MAR = SP = SP - 1; rd
istore4                                  { Blank }
istore5         TOS = MDR; goto (MBR1)
```

[10]

(c) Draw a labelled diagram showing Mic-4's 7-stage pipeline. [7]

Question 3

(a) Explain how each of the following might improve the performance of a microarchitecture:
(i) Branch prediction
(iii) Speculative execution [6]

(b) Define *spatial* and *temporal* locality and explain their relevance to caching. [4]

(c) Draw a labelled diagram of a 2-way set-associative cache with 8 entries. Explain the work done in order to determine whether a given memory addressed is present in this cache. [6]

(d) Distinguish between *write-though* and *write-back* caches. [2]

(e) A direct mapped cache has 32 lines. Each cache line holds 128 bytes. Given that memory addresses in this system are 16 bits long, work out:
(i) The length of the Tag field.
(ii) The line number corresponding to memory address 0xFACE. [2]

Question 4

(a) Describe what is meant by Instruction Set Architecture (ISA). In addition briefly describe any 3 sections you would expect to see in an ISA specification document. [5]

(b) Explain one advantage and one disadvantage of the ASCII system compared with Unicode. [2]

(c) Define any 5 addressing modes. [5]

(d) Design an instruction set format for an architecture with a 21-bit instruction word. Each register operand must be encoded in 6 bits, and each address operand in 10 bits. There are 3 kinds of instructions:

- 2 instructions take 3 register operands.
- 6 instructions take 1 register operand and 1 address operand.
- 256 instructions take 1 address operand. [8]

Question 5

(a) Explain how REPEAT-UNTIL and IF-THEN-ELSE control structures (provided by high level languages such as Pascal) can be written in IJVM assembly language. Give code examples in IJVM assembly language to illustrate your answer. [7]

(b) (i) Outline the main steps carried out by a *two-pass* assembler. [7]

(ii) Describe the structure of the symbol table and explain how it is used for computing branch offsets. [6]

Question 6

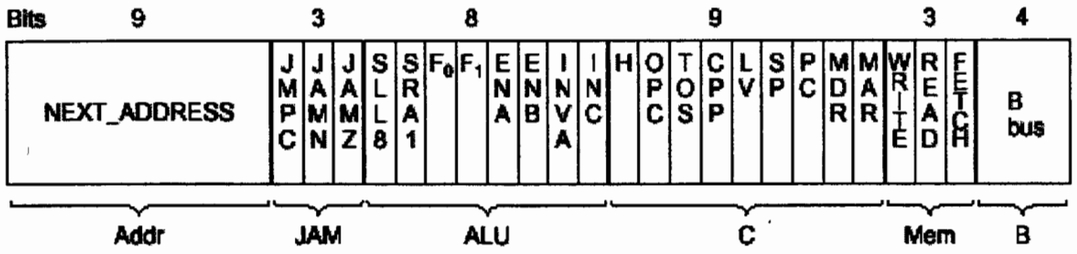
(a) Flynn's taxonomy identifies 4 kinds of computers: SISD, SIMD, MISD and MIMD. Describe the main characteristics of each group. In addition, classify clusters-of-workstations (COWs) and vector processors using Flynn's taxonomy. [8]

(b) Draw diagrams of the following processor-interconnection topologies: *star, tree, ring, grid* and *torus*. In addition, state the diameter of each topology. [10]

(c) State Amdahl's law and briefly explain what it tells us about the limits of parallel computer performance. [2]

Appendix – Microarchitecture & Instruction Set Datasheet

(Source: Andrew S. Tanenbaum, Structured Computer Organization, 5th ed., Prentice-Hall,)



B bus registers

0 = MDR
1 = PC
2 = MBR
3 = MBRU
4 = SP
5 = LV
6 = CPP
7 = TOS
8 = OPC
9-15 none

F_0	F_1	ENA	ENB	INVA	INC	Function
0	1	1	0	0	0	A
0	1	0	1	0	0	B
0	1	1	0	1	0	$\overline{A}$
1	0	1	1	0	0	$\overline{B}$
1	1	1	1	0	0	A + B
1	1	1	1	0	1	A + B + 1
1	1	1	0	0	1	A + 1
1	1	0	1	0	1	B + 1
1	1	1	1	1	1	B – A
1	1	0	1	1	1	B – 1
1	1	1	0	1	1	–A
0	0	1	1	0	0	A AND B
0	1	1	1	0	0	A OR B
0	1	0	0	0	0	0
0	1	0	0	0	1	1
0	1	0	0	1	0	–1

Hex	Mnemonic
0x10	BIPUSH *byte*
0x59	DUP
0xA7	GOTO *offset*
0x60	IADD
0x7E	IAND
0x99	IFEQ *offset*
0x9B	IFLT *offset*
0x9F	IF_ICMPEQ *offset*
0x84	IINC *varnum const*
0x15	ILOAD *varnum*
0xB6	INVOKEVIRTUAL *disp*
0x80	IOR
0xAC	IRETURN
0x36	ISTORE *varnum*
0x64	ISUB
0x13	LDC_W *index*
0x00	NOP
0x57	POP
0x5F	SWAP
0xC4	WIDE