University of Swaziland

Department of Computer Science

Final Examination

May 2012

TITLE OF PAPER:	COMPUTER ORGANISATION I
COURSE NUMBER:	CS 241
TIME ALLOWED:	3 HOURS
INSTRUCTIONS:	ANSWER QUESTION **ONE** FROM **SECTION A** **AND** **ANY THREE** QUESTIONS FROM **SECTION B**

This examination paper should not be opened until the invigilator grants permission.

SECTION A

Question 1 (COMPULSORY)

A. Describe the concept of virtual machine. [2]

B. What is the difference between a translator and interpreter? [2]

C. Draw a clearly labelled diagram of the CPU including control communications. [4]

D. Explain Moore's Law usingprocessor speed as an example. [2]

E. Draw and label the data path of a typical Von Neumann Machine. [3]

F. Illustrate the problem of transferring data from a Big endian machine to a Little endian machine using the integer 260. [2]

G. What is the major problem with a *direct-mapped* cache memory? Describe one of the other cache organisations and say why it does notsuffer from the same problem. [10]

SECTION B (ANSWER ANY THREE QUESTIONS FROM THIS SECTION)

Question 2

A. Convert the following number 123_{10} into the given radices:

   i. Hex [1]

   ii. Two's complement [1]

B. Perform addition on the following sets of binary numbers using one's and two's complement

   i. 1010, 11001 [4]

C. Prove that $(m+ r +1) \leq 2^r$ determines the limit of check bits needed to correct single errors. [5]

D. What is the percentage of bits wasted for the following word sizes: 32, 128, 512. [4]

E. Construct the Hamming code for the following memory word 1111000010101110.[4]

F. Illustrate how this code can correct 2 single bit errors. [6]

Question 3

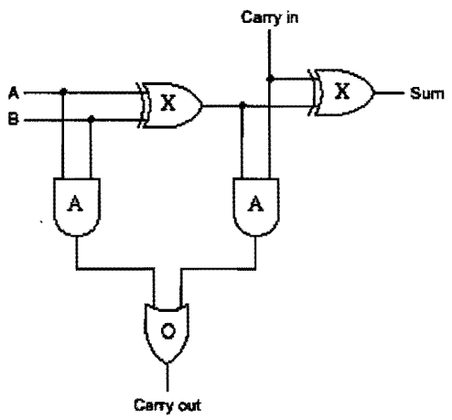
A. Define the locality principle of memory references. [2]

B. Define cache hit ratio, miss ratio. [2]

C. Consider the operation of a machine with the basic Von Neumann data path. Suppose that loading the ALU input registers takes 5 nsec, running the ALU takes 10 nsec, and storing the result back in the register scratchpad takes 5 nsec. What is the maximum number of MIPS this machine is capable of in the absence of pipelining? [4]

D. Describe with the aid of a diagram, Raid 1. [4]

E. What is meant by a superscalar architecture? What are the two types of superscalar machines? [5]



The above cirucit diagram shows a *full adder*. Write out a truth table showing values of the *sum* and *carry out* for all the possible combinations of *A*, *B* and *carry in*.

The gates marked *X* are exclusive or (XOR) gates; those marked *A* are AND gates; the gate marked *O* is an OR. [8]

Question 4

A. Briefly describe the following storage devices:

Flash Disk, DVD [4]

B. Distinguish between synchronous and asynchronous buses [5]

C. Give brief definitions/ descriptions of the following:

i) Modulation [2]

ii) Baud [2]

iii) Duplex channel [2]

D. Describe briefly how register renaming works [2]

E. Describe with the aid of an illustration:

i) Multiplexer [4]

ii) SR latch [4]

Question 5

A. How long does it take to read a disk with 10,000 cylinders, each containing four track of 2048 sectors? First, all sectors of track 0 are to be read starting at sector 0, then all sectors of track 1 starting at sector 0, and so on. The rotation time is 10msec, and a seek takes 1msec between adjacent cylinders and 20 msec for the worst case. Switching between tracks of a cylinder can be done instantaneously. [10]

B. To be able to fit 133 minutes worth of video on a single-sided single-layer DVD, a fair amount of compression is required. Calculate the compression factor required. Assume that 3.5 GB of space is available for the video track, that the image resolution is 720 x 480 pixels with 24-bit color, and images are displayed at 30 frames /sec. [8]

C. Define speculative execution. [3]

D. Describe with relevant illustrations, branch prediction, clearly distinguishing dynamic from static branching. [4]