University of Swaziland

Department of Computer Science

Final Examination

May 2013

TITLE OF PAPER:	COMPUTER ORGANISATION I
COURSE NUMBER:	CS 241
TIME ALLOWED:	3 HOURS
INSTRUCTIONS:	ANSWER QUESTION **ONE** FROM **SECTION A** ANSWER **THREE** QUESTIONS FROM **SECTION B**

This examination paper should not be opened until the invigilator grants permission.

SECTION A

QUESTION 1 (COMPULSORY)

A. Describe the concept of virtual machine. [2]

B. What is the difference between a translator and interpreter? [2]

C. Draw a clearly labelled diagram of the CPU including control communications. [6]

D. Draw and label the typical data path of a typical Von Neumann Machine. [3]

E. What is the difference between a single and multi-cycle datapath? [2]

F. What is the major problem with a *direct-mapped* cache memory? Describe one of the other cache organisations and say why it does notsuffer from the same problem. [10]

SECTION B (ANSWER ANY THREE QUESTIONS FROM THIS SECTION)

QUESTION 2

A. Convert the unsigned number 101101 (base two) to decimal form. [2]

B. Convert the twos complement number 101110 to decimal form [2]

C. Perform addition on the following sets of binary numbers using one's and two's complement

   i. 1010, 11001 [4]

D. Prove that $(m+ r +1) \leq 2^r$ determines the limit of check bits needed to correct single errors. [5]

E. Using the Hamming inequality in (C), What is the percentage of overhead bits for each of the following word sizes: 32, 128, 512, 1024. [4]

F. Construct the Hamming code for the following memory word 1101000010101110.[4]

G. Illustrate how this code can correct 2 single bit errors. [4]

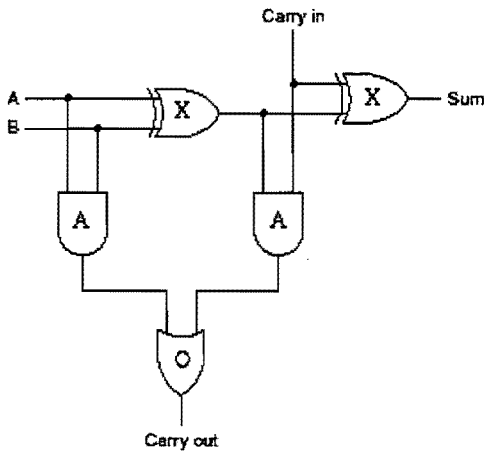
QUESTION 3

A. Explain the locality principle of memory references. How does it influence the memory hierarchy design? [4]

B. Define cache hit ratio, miss ratio, illustrating with the relevant equation [4]

C. Consider the operation of a machine with the basic Von Neumann data path. Suppose that loading the ALU input registers takes 5 nsec, running the ALU takes 10 nsec, and storing the result back in the register scratchpad takes 5 nsec. What is the maximum number of MIPS this machine is capable of in the absence of pipelining? [4]

D. Describe with the aid of a diagram how pipelining works? [5]



The above cirucit diagram shows a *full adder*. The gates marked *X* are exclusive or (XOR) gates; those marked *A* are AND gates; the gate marked *O* is an OR. Write out a truth table showing values of the *sum* and *carry out* for all the possible combinations of *A*, *B* and *carry in*. [8]

QUESTION 4

A. Why are the read and write control lines in a DMA controller should be bidirectional? Under what condition and for what purpose are they used as inputs and as outputs?[4]

B. Distinguish between synchronous and asynchronous buses [5]

C. Give brief definitions/ descriptions of the following:

i) Modulation [2]

ii) Baud [2]

iii) Duplex channel [2]

D. Describe briefly how register renaming works [2]

E. Describe with the aid of an illustration:

i) Multiplexer [4]

ii) SR latch [4]

QUESTION 5

A. How long does it take to read a disk with 10,000 cylinders, each containing four tracks of 2048 sectors? First, all sectors of track 0 are to be read starting at sector 0, then all sectors of track 1 starting at sector 0, and so on. The rotation time is 8msec, and a seek takes 1msec between adjacent cylinders and 20 msec for the worst case. Switching between tracks of a cylinder can be done instantaneously. [5]

B. Describe how register renaming works using a suitable diagram [5]

C. To be able to fit 133 minutes worth of video on a single-sided single-layer DVD, a fair amount of compression is required. Calculate the compression factor required. Assume that 3.5 GB of space is available for the video track, that the image resolution is 720 x 480 pixels with 24-bit color, and images are displayed at 30 frames /sec. [8]

D. Define cycle stealing [3]

E. What is Moore's Law, and why is it important? What is the likelihood that it will hold in the future? Explain in detail. [4]