UNIVERSITY OF SWAZILAND

Faculty of Science

Department of Computer Science

MAIN EXAMINATION December 2012

Title of paper: COMPUTER ORGANISATION II

Course number: CS341

Time allowed: 3 hours

Instructions to candidates:

This question paper consists of **FIVE (5)** questions. Answer any **FOUR (4)** questions. Marks are indicated in the square brackets.

All questions carry equal marks.

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QUESTION 1

a) State 3 differences between Computer Architecture and Computer Organization. [3]

b) What is the purpose of the Microarchitecture level? [3]

c) What do you understand by the term Datapath? What is its function? Describe briefly the 2 basic components of the MIC-1 Datapath. [6]

d) Signals to control the Mic-1 datapath are put into groups. How many groups are they? What modification of the design can be done to reduce the number of control signals for bus B? [6]

e) Briefly explain how the concept of speculative execution is useful in improving performance. [2]

f) Describe the effects of the following lines of Mic-1 microcode: [5]

i. Main Interpreter loop microinstruction.

```
Main1       PC = PC + 1; fetch; goto (MBR)
```

ii. Microinstructions for implementing the ISTORE instruction.

```
ISTORE  H=LV
        MAR=MBRU+H
        MDR=TOS; wr
        SP=MAR=SP-1; rd
        PC=PC+1; fetch
        TOS=MDR; goto Main
```

QUESTION 2

a) The current stack is shown in Fig. 1 The content of SP is 0xFFB00012. What does stack change after executing ISUB instruction? What are values in SP, MDR, H, MAR, TOS? What are the memory addresses of top two words in stack?
Note: The microinstructions for ISUB are as follows. [6]

isub1 MAR=SP=SP-1;rd
isub2 H=TOS
isub3 MDR=TOS=MDR-H; wr; goto Main1

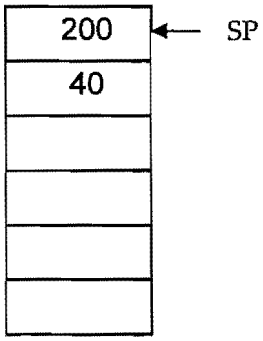

Fig. 1 Stack

b) Given the following lines of code, explain what operation is being implemented:

```
MAR = SP - 1: rd
MAR = SP
H = MDR; wr
MDR = TOS
MAR = SP - 1: wr
TOS = H; goto Main1
```

[5]

c) With the aid of a well labeled diagram and or illustration briefly describe the IJVM memory model. [8]

d) Given the IJVM mnemonics code below. Explain what the code is supposed to do. Rewrite the code in hexadecimal format. [6]

```
BIPUSH 12
ISTORE i
BIPUSH 4
ISTORE j
ILOAD i
ILOAD j
IADD
ISTORE n
```

NB: The IJVM Instruction set is attached at the end of the question paper

QUESTION 3

a) Compute the Boolean expression **(A** AND **B)** OR **C** for [6]

A = 1101 0000 1010 1101
B = 1111 1111 0000 1111
C = 0000 0000 0010 0000

b) Convert into reverse polish notation the following infix expression, (where operators have their usual/normal precedence). $((3+4)*5+3)/(8/2-2)$
Write the IJVM code to evaluate the expression. For every step during the evaluation, show the status of results on the Stack. [10]

c) Evaluate the following reverse polish expression, where each number is a (decimal) digit. $xy+z*a+bc+d+/$ [5]

d) Briefly explain how the Instruction Fetch Unit can help reduce the load on the ALU. [4]

QUESTION 4

a) i) Explain in detail the principle of pipelining, in particular explain how it enhances the performance of a processor. Give an overview of the Six stage pipeline of picoJava II. [9]

ii) Consider a sequence of eight instructions that pass through a four and a six stage pipeline respectively. In which case is the execution time of the sequence shorter? Can we conclude that an increasing number of stages always provides increasing performance? [8]

b) Why is the concept of Branch Prediction important? Briefly describe the strategies of Static and Dynamic Branch prediction. [8]

QUESTION 5

a) Give the IJVM code to evaluate the following expression to calculate the perimeter of a rectangle: P = 2 (A + B) , where A and B are the dimensions (length and width). Assume A and B are assigned the values 3 and 8 respectively. Also use diagrams to show what will be happening on the stack. [8]

b) What does the hypothetical machine instruction ADD [R2], [R3], R1 do? [3]

c) What is the main purpose of the sequencer and the control store? [4]

d) What is the data hazard/dependency in a pipelined system and how can its effects be overcome? [4]

e) Describe the immediate, direct and indirect addressing modes. [6]

The IJVM Instruction Set

Hex	Mnemonic	Meaning
0x10	BIPUSH *byte*	Push byte onto stack
0x59	DUP	Copy top word on stack and push onto stack
0xA7	GOTO *offset*	Unconditional branch
0x60	IADD	Pop two words from stack; push their sum
0x7E	IAND	Pop two words from stack; push Boolean AND
0x99	IFEQ *offset*	Pop word from stack and branch if it is zero
0x9B	IFLT *offset*	Pop word from stack and branch if it is less than zero
0x9F	IF_ICMPEQ *offset*	Pop two words from stack; branch if equal
0x84	IINC *varnum const*	Add a constant to a local variable
0x15	ILOAD *varnum*	Push local variable onto stack
0xB6	INVOKEVIRTUAL *disp*	Invoke a method
0x80	IOR	Pop two words from stack; push Boolean OR
0xAC	IRETURN	Return from method with integer value
0x36	ISTORE *varnum*	Pop word from stack and store in local variable
0x64	ISUB	Pop two words from stack; push their difference
0x13	LDC_W *index*	Push constant from constant pool onto stack
0x00	NOP	Do nothing
0x57	POP	Delete word on top of stack
0x5F	SWAP	Swap the two top words on the stack
0xC4	WIDE	Prefix instruction; next instruction has a 16-bit index