University of Swaziland

Department of Computer Science

Final Examination

May 2014

TITLE OF PAPER:	COMPUTER ORGANISATION I
COURSE NUMBER:	CS 241
TIME ALLOWED:	3 HOURS
INSTRUCTIONS:	ANSWER **ONE** QUESTION FROM **SECTION A** ANSWER **THREE** QUESTIONS FROM **SECTION B**

This examination paper should not be opened until the invigilator grants permission.

SECTION A

QUESTION 1 – 25 MARKS (COMPULSORY)

A. Explain with the aid of diagrams the layered organisation of machine levels [4]

B. What is the difference between translation and interpretation? [2]

C. Explain Moore's Law using processor speed as an example [4]

D. Draw and label the data path of a typical Von Neumann Machine [6]

E. Illustrate the problem of transferring data from a Big endian machine to a Little endian machine using the integer 260. [4]

F. Discuss 3 principles to be considered during the design of an architecture of a CPU [5]

SECTION B (ANSWER ANY THREE QUESTIONS FROM THIS SECTION)

QUESTION 2 – 25 MARKS

A. Convert the following number 654_{10} into the given radices:

i. Hex [2]

ii. Two's complement [2]

B. Prove that $(m+ r +1) \leq 2^r$ determines the limit of check bits needed to correct single errors. [4]

C. Construct the Hamming code for the following memory word 111100001 [4]

D. How can this code correct an error on bit 4. [2]

E. Describe the principle that makes cache memory to be effective [2]

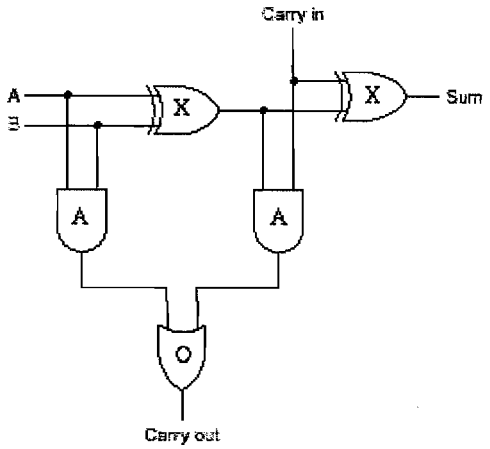
F. What is the major problem with a *direct-mapped* cache memory? Describe one of the other cache organisations and say why it does not suffer from the same problem. [2]

G. Consider the operation of a machine with the basic Von Neumann data path. Suppose that loading the ALU input registers takes 5 nsec, running the ALU takes 10 nsec, and storing the result back in the register scratchpad takes 5 nsec. What is the maximum number of MIPS this machine is capable of in the absence of pipelining? [4]

H. With the aid of a diagram, describe 2 differences between Raid level 0 and Raid level 1 [3]

QUESTION 3 – 25 MARKS

A) Devise a 7 bit hamming code for the numbers from 0 to 8. [5]



The above circuit diagram shows a *full adder*. The gates marked *X* are exclusive or (XOR) gates; those marked *A* are AND gates; the gate marked *O* is an OR.

Write out a truth table showing values of the *sum* and *carry out* for all the possible combinations of *A*, *B* and *carry in*. [10]

B) Disk performance is determined by a number of factors. What is the effect of the following:

a. Latency [3]

b. Seek time [3]

c. Number of Cylinders [2]

d. Sector size [2]

QUESTION 4 - 25 MARKS

a) Briefly describe the following storage devices:
CDROM, DVD [2]

b) Distinguish between synchronous and asynchronous buses [6]

c) Give brief definitions/ descriptions of the following:
i) Modulation [2]
ii) Baud [2]
iii) Duplex channel [2]

d) Describe briefly how ADSL works [3]

e) Identify character Codes [2]

f) Describe with the aid of an illustration:
i) Multiplexer [3]
ii) Decoder [3]

QUESTION 5 – 25 MARKS

A. How long does it take to read a disk with 10,000 cylinders, each containing four track of 2048 sectors? First, all sectors of track 0 are to be read starting at sector 0, then all sectors of track 1 starting at sector 0, and so on. The rotation time is 10msec, and a seek takes 1msec between adjacent cylinders and 20 msec for the worst case. Switching between tracks of a cylinder can be done instantaneously. [8]

B. To be able to fit 133 minutes worth of video on a single-sided single-layer DVD, a fair amount of compression is required. Calculate the compression factor required. Assume that 3.5 GB of space is available for the video track, that the image resolution is 720 x 480 pixels with 24-bit color, and images are displayed at 30 frames /sec. [8]

C. Describe with relevant illustrations, branch prediction, clearly distinguishing dynamic from static branching. [7]

END OF EXAM ---------- ---------- TOTAL: 100 MARKS