# University of Swaziland 

Department of Computer Science
Final Examination
DECEMBER 2013
TITLE OF PAPER: COMPUTER ORGANISATION II
COURSE NUMBER: ..... CS 341
TIME ALLOWED: 3 HOURS
INSTRUCTIONS: ANSWER ONE QUESTION FROM SECTION AANSWER THREE QUESTIONS FROM SECTION B

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## SECTION A

## QUESTION 1 (COMPULSORY)

A) An instruction set has 4 bits for opcode and 32 bits for addresses. What percentage change in instructions and memory resolution results if the opcode is increased by 2 bits without altering the instruction length (by taking bits from address portion).
B) Identify the addressing mode described by the features below:
i). The data is part of the instruction. A constant. This can be combined with other addressing modes.
ii). The data we need is in memory. A register contains the address of the data. We specify a register. The register is a pointer to memory.
iii). The data we need is in memory. A register contains an address. The data is at a known offset from the address. We specify a register and an offset.
C) What is addressing orthorgonality?
D) Convert the infix formula $(a+c d+7) / x+c y-4)$ to postfix
E) Create a bit-map for the disk shown in (b) below. Occupied blocks are marked with a number.

(a)

(b)

## SECTION B (ANSWER ANY THREE QUESTIONS FROM THIS SECTION)

## QUESTION 2

A) Describe the $\mathbf{3}$ differences between programmed I/O and Interrupt driven I/O
B) Given memory partitions of $100 \mathrm{~K}, 500 \mathrm{~K}, 200 \mathrm{~K}, 300 \mathrm{~K}$, and 600 K (in order), how would each of the First-fit, Best-fit, and Worst-fit algorithms place processes of $212 \mathrm{~K}, 417 \mathrm{~K}$, 112 K , and 426 K (in order)? Which algorithm makes the most efficient use of memory?
C) Assume you have an expanding opcode that supports the following formats, with a 3 bit register:

4 instructions with 3 registers
255 instructions with one register
16 instructions with zero registers
i. How many opcodes, in total, does the preceding require?
ii. How many bits does the opcode require to support the 3 formats?
D) Explain, using a suitable illustration, how semaphores work

## QUESTION 3

a) A program takes 10 months to write in a high level language and takes 100 seconds to complete it's task. Two modules are responsible for $30 \%$ and $20 \%$ of the execution time of the program, respectively. These modules are of roughly equal complexity and account for $10 \%$ (each) of the total development effort. The compiler used can produce symbolic assembly language, so it only takes twice as long to tune the assembly language version as it took to write it initially. The anticipated speed up is a factor of two for each module.
i. Can both modules be optimized prior to the one year ship date (two more months)?
ii. What is the anticipated execution time after the tuning has been performed? (even if it is past the deadline)
b) Syntax and Semantic error messages refer to source code line numbers.
i. How are these numbers affected by Macro Expansion?
ii. Should error messages be produced during the first pass or the second pass? Explain you answer.
c) Describe static binding giving an advantage and a disadvantage.

## QUESTION 4

Describe in not more than 80 words each, using correct terminology and illustrations:
A) Segmentation.
B) Paging.
C) Paged segmentation.

## QUESTION 5

a) Using Amdahl's law on a given program which has $50 \%$ sequential code and $50 \%$ parallel:
i. What is the speed up anticipated with two processors?
ii. What about 4 processors?
iii. How many processors would result in a 4 -fold speedup?
b) Four (4) CPUs are connected by a bus whose bandwidth is $r \mathrm{MB} / \mathrm{sec}$, by what percentage has the bandwidth changed if the system is scaled to 22 CPUs.
c) Suppose that for technical reasons it is only possible for a snooping cache to snoop on the address lines, not data lines. Would this change affect the write through protocol? [6]

