UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF COMPUTER SCIENCE

MAIN EXAMINATION - MAY 2015

TITLE OF PAPER:	**COMPUTER ORGANIZATION I**
COURSE NUMBER:	**CS 241**
TIME ALLOWED:	**3 HOURS**
INSTRUCTIONS:	**ANSWER QUESTION 1 FROM SECTION A** **ANSWER ANY 3 QUESTIONS FROM SECTION B**

This examination paper should not be opened until the invigilator grants permission.

SECTION A

QUESTION 1 (COMPULSORY – 25 MARKS)

A. Explain with the aid of diagrams the layered organisation of machine levels [4]

B. What is the difference between translation and interpretation? [2]

C. Explain Moore's Law with an example from each of the following:

i. Number of transistors in a CPU [2]
ii. Memory capacity [2]

D. Draw and label the data path of a typical Von Neumann Machine. [6]

E. Illustrate the problem of transferring data from a Big endian machine to a Little endian machine using the integer 260. [4]

F. Discuss 3 principles to be considered during the design of an architecture of a CPU. [5]

SECTION B (ANSWER ANY *THREE* QUESTIONS FROM THIS SECTION)

QUESTION 2 (25 MARKS)

A. The inequality $(\mathbf{m + r + 1}) \leq 2^{\mathbf{r}}$ determines the limit of the check bits needed to correct all single-bit errors.

i. Create a table for the hamming codes for the following message sizes indicating: message length, codeword length, number of check bits and the percentage of bits wasted for the following word sizes: 8, 16, 64, 256, 512. [15]

ii. Construct the Hamming code for the following 16-bit message 1111000010101110. [5]

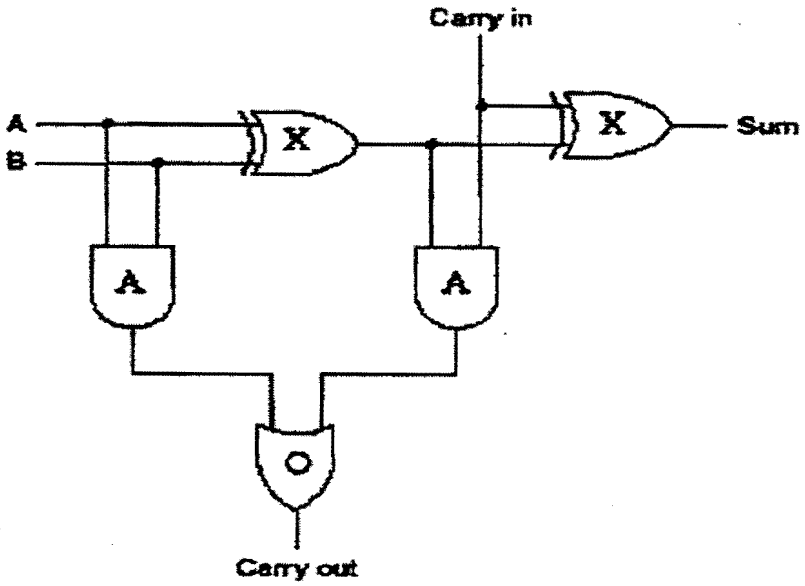
B. Define the principle that determines the success of the cache memory. [3]

C. Define cache hit ratio and cache miss ratio. [2]

QUESTION 3 (25 MARKS)

A. Draw a half adder. [5]

B. Describe a multiplexer with the aid of a diagram. [5]



C. The above circuit diagram shows a full adder. Write out the truth table showing values of the *sum* and *carry out* of all the possible combinations of *A*, *B* and *carry in*.

The gates marked X are exclusive or (XOR) gates; those marked *A* are AND gates; the gate marked 0 is an OR. [10]

D. Describe with the aid of a diagram how pipelining works? [5]

QUESTION 4 (25 MARKS)

A. Distinguish between synchronous and asynchronous buses [9]

B. Describe with the aid of an illustration:

i) Decoder [8]
ii) SR latch [8]

QUESTION 5 (25 MARKS)

A. Consider a disk that rotates at 3600 rpm. The seek time to move the head between adjacent tracks is 2ms. There are 32 sectors per track, which is stored in linear order from sector 0 through sector 31. The head sees the sectors in ascending order. Assume the read/write head is positioned at the start of sector 1 on track 8. There is a main memory buffer large enough to hold an entire track. Data is transferred between disk locations by reading from the source track into the main memory buffer and then writing the data from the buffer to the target track.

   a. How long will it take to transfer sector 1on track 8 to sector 1 on track 9? [7]

   b. How long will it take to transfer all sectors of track 8 to the corresponding sectors of track 9? [5]

B. With an aid of a diagram, illustrate the memory hierarchy. Explain the three key parameters that increase as you move down the hierarchy. [6]

C. Define speculative execution. [3]

D. Describe with relevant illustrations, branch prediction, clearly distinguishing dynamic from static branching. [4]

END OF PAPER!