UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF COMPUTER SCIENCE

SUPPLEMENTARY EXAMINATION
JULY 2015

TITLE OF PAPER: COMPUTER ORGANIZATION I

COURSE NUMBER: CS 241

TIME ALLOWED: 3 HOURS

INSTRUCTIONS: ANSWER QUESTION 1 FROM SECTION A
                          ANSWER ANY 3 QUESTIONS FROM SECTION B

This examination paper should not be opened until the invigilator grants permission.

SECTION A

QUESTION 1 (COMPULSORY)

A. Describe the concept of virtual machine.   [2]

B. What is the difference between a translator and interpreter?   [2]

C. Draw a clearly labelled diagram of the CPU including control communications. [5]

D. Explain the locality principle of memory references. How does it influence the memory hierarchy design?   [4]

E. Define cache hit ratio, miss ratio, illustrating with the relevant equation   [4]

F. Describe with the aid of a diagram how pipelining works?   [5]

G. What is Moore's Law, and why is it important? What is the likelihood that it will hold in the future? Explain in detail.   [3]

SECTION B (ANSWER ANY *THREE* QUESTIONS FROM THIS SECTION)

QUESTION 2 (25 MARKS)

A. Prove that $(m + r + 1) \leq 2^r$ determines the limit of check bits needed to correct single errors. [5]

B. What is the percentage of bits wasted for the following word sizes: 32, 128, 512. [4]

C. Construct the Hamming code for the following memory word 1010001110110101. [5]

D. Illustrate how this code can correct 2 single bit errors. [6]

E. What is meant by a superscalar architecture? What are the two types of superscalar machines? [5]

QUESTION 3 (25 MARKS)

A. Distinguish between synchronous and asynchronous buses [6]

B. Write short notes on any 2 of the following; [10]

      (a) fetch – decode – execute cycle
      (b) cache memory
      (c) pipelining

C. Briefly describe the following storage devices: CDROM, DVD   [5]

D. What is the difference between the following:
   - bus master and slave   [4]

QUESTION 4 (25 MARKS)

A. Draw a circuit showing 2 transistors connected together to form a NOR gate.   [3]

B. Draw the following logic circuits;

- 3-bit comparator   [3]
- 4-bit multiplexer   [6]
- 3-to-8 decoder   [6]

C. Draw a circuit diagram of a 1-bit left/right shifter. It must input a 4-bit value   [7]

QUESTION 5 (25 MARKS)

A. Consider a disk that rotates at 3600 rpm. The seek time to move the head between adjacent tracks is 2ms. There are 32 sectors per track, which is stored in linear order from sector 0 through sector 31. The head sees the sectors in ascending order. Assume the read/write head is positioned at the start of sector 1 on track 8. There is a main memory buffer large enough to hold an entire track. Data is transferred between disk locations by reading from the source track into the main memory buffer and then writing the data from the buffer to the target track.

    a. How long will it take to transfer sector 1 on track 8 to sector 1 on track 9? [7]

    b. How long will it take to transfer all sectors of track 8 to the corresponding sectors of track 9? [5]

B. With an aid of a diagram, illustrate the memory hierarchy. Explain the three key parameters that increase as you move down the hierarchy. [6]

C. Define speculative execution. [3]

D. Describe with relevant illustrations, branch prediction, clearly distinguishing dynamic from static branching. [4]

END OF PAPER!