**University of Swaziland**

# *Department of Computer Science*

Supplementary Examination

**July 2015**

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| TITLE OF PAPER: | COMPUTER ORGANISATION II |
| COURSE NUMBER: | CS 341 |
| TIME ALLOWED: | 3 HOURS |
| INSTRUCTIONS: | ANSWER **ONE** QUESTION FROM **SECTION A**<br>ANSWER **THREE** QUESTIONS FROM **SECTION B** |

This examination paper should not be opened until the invigilator grants permission.

## SECTION A

## QUESTION 1 (COMPULSORY)

A) An instruction set has 4 bits for *opcode* and 32 bits for addresses. What percentage change in instructions and memory resolution results if the *opcode* is increased by 2 bits without altering the instruction length (by taking bits from address portion). [4]

B) Identify the *addressing mode* described by the features below:

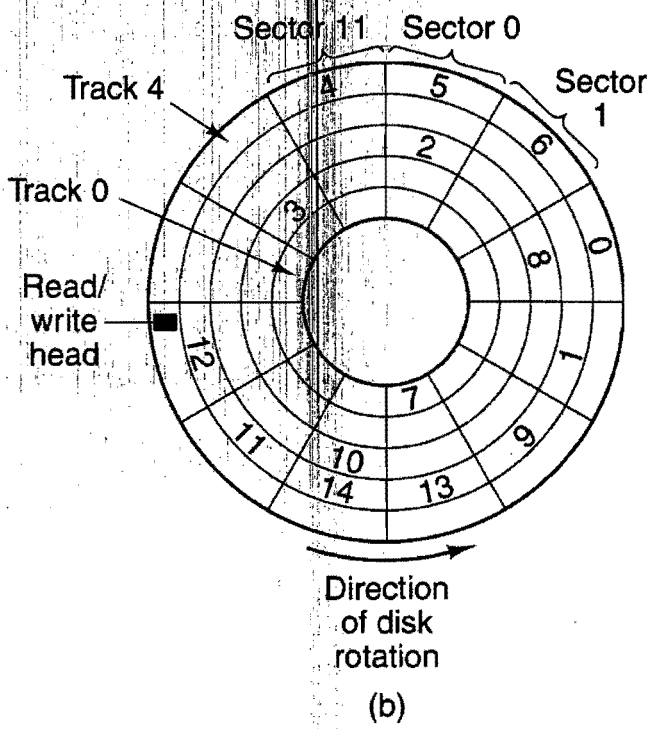
i). The data is part of the instruction. A constant. This can be combined with other addressing modes. [2]

ii). The data we need is in memory. A register contains the address of the data. We specify a register. The register is a pointer to memory. [2]

iii). The data we need is in memory. A register contains an address. The data is at a known offset from the address. We specify a register and an offset. [2]

C) Convert the infix formula (a+cd)/(cy-4) to postfix [5]

D) Create a free-list for the disk shown in (b) below. Occupied blocks are marked with a number. [10]




(b)

## SECTION B (ANSWER ANY THREE QUESTIONS FROM THIS SECTION)

### QUESTION 2

a) Describe the 2 differences between **programmed I/O** and **DMA I/O** [8]

b) Describe, with the aid of diagrams, the following allocation algorithms:
   i. First fit
   ii. Best fit [8]

c) Assume you have an expanding *opcode* that supports the following formats, with a 3 bit register:

   4 instructions with 3 registers
   255 instructions with one register
   16 instructions with zero registers

   i. How many *opcodes*, in total, does the preceding require? [3]
   ii. How many **bits** does the *opcode* require to support the 3 formats? [3]

d) Explain, using a suitable illustration, how semaphores work [4]

### QUESTION 3

Describe, the following, using correct terminology and appropriate illustrations, :

a) Segmentation. [10]
b) Paging. [15]

### QUESTION 4

a) A program takes 10 months to write in a high level language and takes 100 seconds to complete it's task. Two modules are responsible for 30% and 20% of the execution time of the program, respectively. These modules are of roughly equal complexity and account for 10% (each) of the total development effort. The compiler used can produce symbolic assembly language, so it only takes twice as long to tune the assembly language version as it took to write it initially. The anticipated speed up is a factor of two for each module.

   i. Can both modules be optimized prior to the one year ship date (two more months)? [7]
   ii. What is the anticipated execution time after the tuning has been performed? (even if it is past the deadline) [6]

b) Syntax and Semantic error messages refer to source code line numbers.

   i. How are these numbers affected by Macro Expansion? [6]
   ii. Should error messages be produced during the first pass or the second pass? (or can you say?) [6]

## QUESTION 5

a) Using Amdahl's law on a given program which has 50% sequential code and 50% parallel:

i. What is the speed up anticipated with two processors? [5]
ii. What about 4 processors? [4]
iii. How many processors would result in a 4-fold speedup? [4]

b) Four (4) CPUs are connected by a bus whose bandwidth is *r* MB/sec, by what percentage has the bandwidth changed if the system is scaled to 22 CPUs. [6]

c) Suppose that for technical reasons it is only possible for a snooping cache to snoop on the address lines, not data lines. Would this change affect the *write through* protocol? [6]

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END OF EXAM