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UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF COMPUTER SCIENCE

MAIN EXAMINATION - MAY 2016

TITLE OF PAPER:	**COMPUTER ORGANIZATION I**
COURSE NUMBER:	**CS 241**
TIME ALLOWED:	**3 HOURS**
INSTRUCTIONS:	**ANSWER QUESTION 1 FROM SECTION A** **ANSWER ANY 3 QUESTIONS FROM SECTION B**

This examination paper should not be opened until the invigilator grants permission.

SECTION A

Question 1 (COMPULSORY)

A. Describe the concept of virtual machine. [2]

B. What is the difference between a translator and interpreter? [2]

C. Explain Moore's Law using processor speed as an example. [4]

D. Draw and label the data path of a typical Von Neumann Machine. [5]

E. Suppose that the following byte values (shown in hexadecimal) are found in 4 consecutive memory locations starting at address 256:

80 40 02 01

i. What is the 2-byte value at address 258, assuming big-endian representation?

ii. What is the 4-byte value at address 256, assuming little-endian representation?

[2]

F. What is the major problem with a *direct-mapped* cache memory? Describe one of the other cache organisations and say why it does not suffer from the same problem. [10]

SECTION B (ANSWER ANY *THREE* QUESTIONS FROM THIS SECTION)

Question 2

Write short notes on any 5 of the following; [25]

A. Fetch-decode-execute cycle
B. Word size
C. CISC vs RISC
D. Instruction pipelining
E. Memory hierarchy
F. Bus arbitration
G. Superscalar architecture

Question 3

A. Define the locality principle of memory references. [2]

B. Define cache hit ratio, miss ratio. [2]

C. Consider the operation of a machine with the basic Von Neumann data path. Suppose that loading the ALU input registers takes 5 nsec, running the ALU takes 10 nsec, and storing the result back in the register scratchpad takes 5 nsec. What is the maximum number of MIPS this machine is capable of in the absence of pipelining? [4]

D. Describe with the aid of a diagram, Raid 1. [4]

E. Convert the integer 2063 into the following radix:

i. bin, [2]
ii. hex [3]

Question 4

A) Draw a diagram showing a NOR gate constructed using 2 transistors. [4]

B) A chip has 5 input and 32 output pins. The output pins are numbered from 0 to 31. Upon testing, the chip is always seen to output a 1 on pin number X, where X is the input integer; meanwhile 0 is output on all other pins.

i. What is the full name of this device? [1]

ii. What type of logic gates are required to build this device? State how many of each type are needed. [2]

iii. In addition to the 37 pins for data input and output, there are 2 other pins in this chip. Name both pins and state their purpose. [2]

C) Draw a circuit diagram for a 3-bit comparator [3]

D) Draw a circuit diagram for a 4-input multiplexer [5]

E) Construct the Hamming code for the following memory word 1101000010101110. [4]

F) Illustrate how this code can correct 2 single bit errors. [4]

Question 5

A. Consider a disk that rotates at 3600 rpm. The seek time to move the head between adjacent tracks is 2ms. There are 32 sectors per track, which is stored in linear order from sector 0 through sector 31. The head sees the sectors in ascending order. Assume the read/write head is positioned at the start of sector 1 on track 8. There is a main memory buffer large enough to hold an entire track. Data is transferred between disk locations by reading from the source track into the main memory buffer and then writing the data from the buffer to the target track.

   a. How long will it take to transfer sector 1on track 8 to sector 1 on track 9? [7]

   b. How long will it take to transfer all sectors of track 8 to the corresponding sectors of track 9? [5]

B. With an aid of a diagram, illustrate the memory hierarchy. Explain the three key parameters that increase as you move down the hierarchy. [6]

C. Define speculative execution. [3]

D. Describe with relevant illustrations, branch prediction, clearly distinguishing dynamic from static branching. [4]

END OF PAPER!