

Question 1

- A. Illustrate the problem of transferring data from a Big endian machine to a Little endian machine using the integer 260. [4]
- B. A chip has 5 input and 32 output pins. The output pins are numbered from 0 to 31. Upon testing, the chip is always seen to output a 1 on pin number X, where X is the input integer; meanwhile 0 is output on all other pins.
- i. What is the full name of the device? [1]
 - ii. What type of logic gates are required to build this device? State how many of each they are needed. [2]
 - iii. In addition to the 37 pins for data input and output, there are 2 other pins in this chip. Name both pins and state their purpose. [2]
- C. Draw a circuit diagram of a 3-bit comparator. [3]
- D. Draw a circuit diagram of a 4-input multiplexer. [5]
- E. Draw a circuit diagram of a subtraction circuit that input two 4-bit integers, X and Y, and outputs their difference, i.e. X-Y. Draw the adders in your diagram in the form of chips. [8]

Question 2

A. Convert the following number 123_{10} into the given radices:

i. Hex [2]

ii. Two's complement [2]

B. Perform addition on the following sets of binary numbers using one's and two's complement

i. 1010, 11001 [2]

C. Prove that $(m + r + 1) \leq 2^r$ determines the limit of check bits needed to correct single errors. [6]

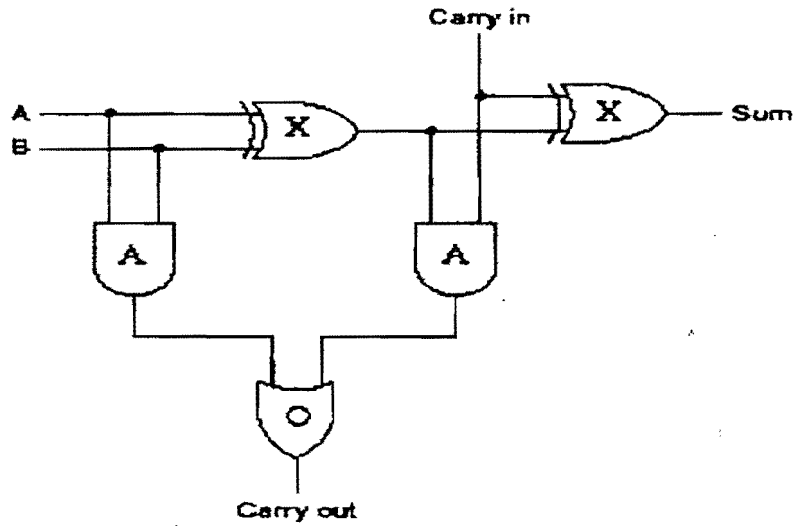
D. What is the percentage of bits wasted for the following word sizes: 32, 128, and 512? [4]

E. Construct the Hamming code for the following memory word 1111000010101110. [6]

F. Illustrate how this code can correct 2 single bit errors. [3]

Question 3

A. What is meant by a superscalar architecture? What are the two types of superscalar machines? [5]



B. The above circuit diagram shows a full adder. Write out the truth table showing values of the *sum* and *carry out* all the possible combinations of *A*, *B* and *carry in*. The gates marked X are exclusive or (XOR) gates; those marked A are AND gates; the gate marked O is an OR. [10]

C. Describe with the aid of a diagram how pipelining works? [5]

D. Describe a multiplexer with the aid of a diagram. [5]

Question 4

A. Why are the read and write control lines in a DMA controller should be bidirectional?

Under what condition(s) and for what purpose are they used as inputs and as outputs? [4]

B. Distinguish between synchronous and asynchronous buses [5]

C. Give brief definitions/descriptions of the following:

i) Modulation [2]

ii) Baud [2]

iii) Duplex channel [2]

D. Describe briefly how register renaming works. [2]

Question 5

- A. Consider a disk that rotates at 3600 rpm. The seek time to move the head between adjacent tracks is 2ms. There are 32 sectors per track, which is stored in linear order from sector 0 through sector 31. The head sees the sectors in ascending order. Assume the read/write head is positioned at the start of sector 1 on track 8. There is a main memory buffer large enough to hold an entire track. Data is transferred between disk locations by reading from the source track into the main memory buffer and then writing the data from the buffer to the target track.
- i) How long will it take to transfer sector 1 on track 8 to sector 1 on track 9? [7]
 - ii) How long will it take to transfer all sectors of track 8 to the corresponding sectors of track 9? [5]
- B. With an aid of a diagram, illustrate the memory hierarchy. Explain the three key parameters that increase as you move down the hierarchy. [6]
- C. Define speculative execution. [3]
- D. Describe with relevant illustrations, branch prediction, clearly distinguishing dynamic from static branching. [4]

END OF PAPER!