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UNIVERSITY OF SWAZILAND

Faculty of Science

Department of Computer Science

MAIN EXAMINATION December 2015

Title of Paper: **COMPUTER ORGANISATION II**

Course Number: **CS341**

Time Allowed: **3 hours** Total Marks: **100**

Instructions to candidates:

*This question paper consists of **FIVE (5)** questions.*

*ANSWER **ONE** QUESTION FROM **SECTION A***
*ANSWER **THREE** QUESTIONS FROM **SECTION B***

All questions carry equal marks.

SPECIAL REQUIREMENTS:

NO CALCULATORS ALLOWED

THIS EXAMINATION PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GRANTED BY THE INVIGILATOR

SECTION A

QUESTION 1 (COMPULSORY)

A) An instruction set has 4 bits for *opcode* and 32 bits for addresses. What percentage change in instructions and memory resolution results if the *opcode* is increased by 2 bits without altering the instruction length (by taking bits from address portion). [4]

B) Compare using the aid of suitable diagrams:

i) multiprocessor and multicomputer [4]
ii). Strict consistency and release consistency [4]
iii). Cache miss and page fault [4]
iv). Conditional and unconditional branching [4]

C) Write the integer 255 in binary notation and in binary coded decimal (BCD). How does this example demonstrate the inefficiency of the BCD? [2]

D) Discuss the advantages and disadvantages of minimizing the length of an instruction format. [3]

SECTION B (ANSWER ANY *THREE* QUESTIONS FROM THIS SECTION)

QUESTION 2

A) Describe what is meant by Instruction Set Architecture (ISA). In addition briefly describe any 3 sections you would expect to see in an ISA specification document. [5]

B) Explain one advantage and one disadvantage of the ASCII system compared with Unicode. [2]

C) Define any 5 addressing modes. [5]

D) Design an instruction set format for an architecture with a 21-bit instruction word. Each register operand must be encoded in 6 bits, and each address operand in 10 bits. There are 3 kinds of instructions:

- 2 instructions take 3 register operands.
- 6 instructions take 1 register operand and 1 address operand.
- 256 instructions take 1 address operand. [8]

QUESTION 3

A) Briefly explain how the concept of speculative execution is useful in improving performance. [5]

B) Evaluate the following arithmetic expression into Decimal.

$$121_{16} + 122_{10} - 123_{8} \quad [5]$$

C) Evaluate the following reverse polish expression, where each number is a (decimal) digit.

ABCDE F /+G -H /* +* [5]

D) Convert into reverse polish notation the following infix expression (where operators have their usual/normal precedence) *(2x* 3 +4)-(4/2 + 1). Generate IJVM code to evaluate it. Show values in the Stack during the evaluation. [10]
*(See the **IJVM** instruction set on last page)*

QUESTION 4

A) Give the IJVM code to evaluate the following expression to calculate the perimeter of a rectangle: P = 2 (A + B), where A and B are the dimensions (length and width). Assume A and B are assigned the values 3 and 8 respectively. Also use diagrams to show what will be happening on the stack. [8]

B) What does the hypothetical machine instruction ADD [R2], [R3], Rl do? [3]

C) What is the main purpose of the sequencer and the control store? [4]

D) What is the data hazard/dependency in a pipelined system and how can its effects be overcome? [4]

E) Describe the immediate, direct and indirect addressing modes. [6]

QUESTION 5

A) Using Amdahl's law on a given program which has 50% sequential code and 50% parallel:

i. What is the speed up anticipated with two processors? [5]
ii. What about 4 processors? [4]

iii. How many processors would result in a 4-fold speedup? [4]

B) Four (4) CPU s are connected by a bus whose bandwidth is *r* MB/sec, by what percentage has the bandwidth changed if the system is scaled to 22 CPUs. [6]

C) Suppose that for technical reasons it is only possible for a snooping cache to snoop on the address lines, not data lines. Would this change affect the *write through* protocol? [6]

<< End of Question Paper >>