University of Eswatini

Department of Computer Science

Final Examination

2018/19

Title of Paper: Computer Architecture & Organisation I

Course Number: CSC222

Time Allowed: Three (3) hours

Instructions: Answer **ALL** questions

You are not allowed to open this paper until you have been told to do so by the invigilator.

Question 1 (25)

SCENARIO

As a Computer Science student at the University of Eswatini, you have been nominated to assist in the upcoming National Universities sports competitions to be hosted at Somhlolo stadium. As part of the preparation for this event there will be meetings held in all the participating universities across the country. All the organizers in each participating university need to set up computer systems to be able to manage and process the vast amount of data that will be obtained from the registration of the athletes as well as the results for each event. Volunteers from the local communities and schools also have offered their assistance.

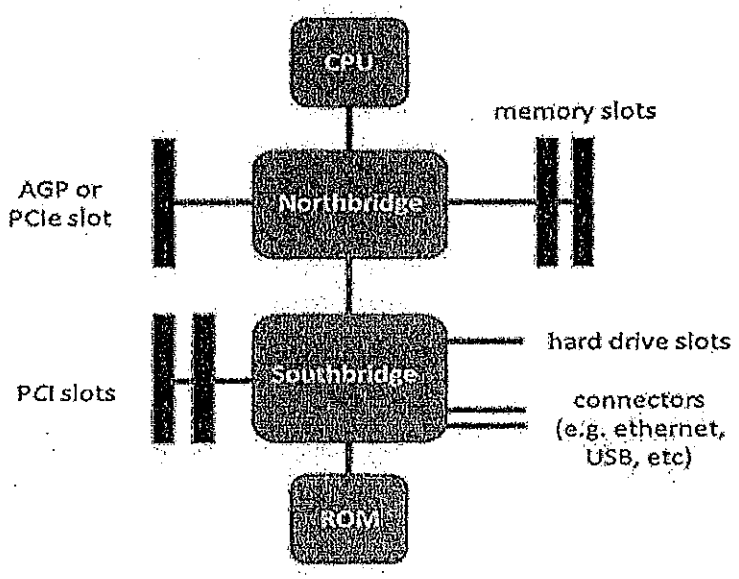


Diagram 1

Diagram 1 represents some of the components of the computer motherboard, as a computer designer you are expected to explain some of the components to the volunteers by answering the following questions

1.1 CPU contains registers. Briefly explain the function of registers. (3)

1.2 Explain why instructions loaded in cache memory are processed faster by the CPU than instructions stored in RAM.
(3)

1.3 The basic process of how a CPU operates consists of four stages, namely fetch, decode, execute and store. Briefly describe what takes place during the DECODE stage. (3)

1.4 What is the physical connection between the CPU and the north bridge called? (2)

1.5 Different slots, such as AGP and PCI Express, are found on a motherboard.

1.5.1 What is the purpose of the AGP slot? (2)

1.5.2 To which bridge (north or south) is an AGP slot connected? (2)

1.6 Someone told the volunteer that the PCI Express slots are on-board and not hot-pluggable.

1.6.1 What does on-board mean?

1.6.2 What does it mean when a device is NOT hot-pluggable? (2)

1.7 All computer systems must have a RAM and ROM.

1.7.1 State TWO major differences between RAM and ROM. (2)

1.7.2 Explain the purpose of ROM. (2)

1.8 Large quantities of data related to all the athletes need to be saved on hard drives (HDD).

1.8.1 Explain two (2) aspects that influence the access time of an HDD. (2)

1.8.2 Disk caching will improve performance in terms of the storage and retrieval of data. Explain what disk caching is. (2)

Question 2 (25)

2.1 I/O devices are used to exchange information between user and CPU. An I/O organization includes two major components namely I/O devices, I/O module. In addition it uses different techniques to exchange information. List and define the three techniques for performing I/O modules from the least efficient to the best performing.
(6)

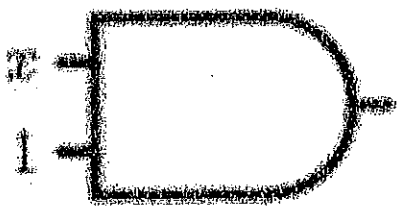
2.2 In some ADC/DAC devices there are options to output/input the data in 2's Complement form.
What are the advantages of representing digital data in 2's Complement form when you can simply have straight binary code and save time of conversion? (5)

2.3 Using 7 bits to represent each number, write the representations of 23 and -23, 10 and -10 in signed Magnitude and 2's complement integers. (6)

	Signed Magnitude	1's Complement	2's Complement
23			
-23			
10			
-10			

2.4 With the help of a flow chart use the Booth's multiplications algorithm to multiply *7X3*. (5)

2.5 Consider the AND gate where one of the inputs is 1. By using the truth table investigate the possible outputs and hence simplify the expression $x \cdot 1$. (3)



Question 3 (25)

3.1 Some processors use memory mapped I/O where I/O devices are in the same address space as main memory. Others have separate I/O address space and separate instructions. Give some advantages and disadvantages of each. (6)

3.2 Although DMA does not use the CPU, the maximum transfer rate is still limited. Consider reading a block from the disk. Name three factors that might ultimately limit the rate transfer. (3)

3.2.1 List and briefly define the key services provided by an OS. (8)

3.2.2 Briefly describe define the major types of OS scheduling. (8)

Question 4 (25)

4.1 The Instruction Set Architecture (ISA) is the part of the processor that is visible to the programmer or compiler writer and serves as the boundary between software and hardware. Briefly describe the 3 most common types of ISAs. (6)

4.2 Each instruction of a computer specifies an operation on certain data. They are various ways of specifying addresses of the data to be operated on. These different ways of specifying data are called the addressing modes.

4.3 Describe in detail the different kinds of addressing modes with an example where possible (9)

What are the main differences between RISC and CISC architectures (5)

4.4 When a device interrupt occurs, how does the processor determine which device issued the interrupt? (5)