UNIVERSITY OF ESWATINI

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF COMPUTER SCIENCE

RESIT EXAMINATION

JANUARY 2019

TITLE OF PAPER: INTRODUCTION TO LOGIC

COURSE CODE: CSC201

TIME ALLOWED: 3 HOURS **TOTAL MARKS: 100**

INSTRUCTIONS TO CANDIDATES:

1. All questions carry equal marks.
2. **Question 1 is compulsory.**
3. Answer any 3 Questions from Question 2 to Question 5.
4. Marks for each question are indicated in square brackets.
5. Show all your workings where necessary.

THIS EXAMINATION PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GRANTED BY THE INVIGILATOR

Question 1

(a) Define the following terms as used in logic. [5]

(i) Clause

(ii) Literal

(iii) Exclusive OR

(iv) Contradiction

(v) Combinational circuit

(b) Draw the truth table of the following proposition. [5]

$$P \wedge \bar{Q} \rightarrow \bar{P} \vee R$$

(c) From the truth table in (b) above, derive the DNF and CNF of the function. [5]

(d) Draw the circuit of the following function using basic logic gates only. [6]

$$\overline{ab.\bar{c} + (a+b)}$$

(e) Convert the following to predicate logic statements.

(i) Some university students are government sponsored and some are self-sponsored. [2]

(ii) All computer science study CSC101 and some computer science students study PHY211. [2]

Question 2

(a) Use truth tables to prove the following

(i) $(P \vee Q) \rightarrow R \cong (P \rightarrow R) \wedge (Q \rightarrow R)$ [5]

(ii) $(P \rightarrow Q) \wedge P \models Q$ [4]

(b) Use laws of logical equivalence to prove the following equivalences.

(i) $(P \vee Q) \rightarrow R \cong (P \rightarrow Q) \wedge (R \rightarrow Q)$ [4]

(ii) $(P \rightarrow Q) \leftrightarrow \neg(P \rightarrow Q)$ is a contradiction [5]

(c) Give advantages of using laws of logical equivalence over the truth table method to prove equivalences. [2]

(d) Give the premises $A \wedge B, A \rightarrow C, B \wedge C \rightarrow D$, prove D. [5]

Question 3

(a) Use the Quine McCluskey method to minimize the following function. [5]

$$f(a,b,c,d) = \sum(3,7,10,11,13,15)$$

(b) Draw the circuit of the reduced function in (a) above. [4]

(c) A digital parity checker takes in a bit input and checks the parity of the input. It returns 0 if the number of 1 is odd in the input and 1 if the number of 1s is even. The case where all inputs are 0s is a don't care condition. Implement the reduced circuit of the parity checker. [12]

(d) Convert the following function to canonical SOP. [4]

$$f(a,b,c) = ab + \bar{c}$$

Question 4

(a) Convert the following function to POS using laws of logical equivalence. [4]

$$f(x,y,z) = \overline{(x+y)} + z$$

(b) Find the canonical POS and canonical SOP of the function in (a) above and represent them in short-hand form. [10]

(c) Explain the difference between a half adder and a full adder. [2]

(d) Use the resolution rule to prove the following. [5]

Premises:

$$(p \wedge q) \vee r$$

$$r \rightarrow s$$

Conclusion:

$$p \vee s$$

(e) Write the following statement in predicate logic syntax using the universal quantifier only. [4]

Everyone has a male and female parent.

Question 5

(a) Define a predicate model. [3]

(b) Write the following statement using predicate logic syntax. [4]

Anyone who loves everyone loves themselves.

(c) Use the K-map method to simplify the expression. [7]

$$f(w,x,y,z) = \bar{w} \cdot \bar{x} \cdot \bar{y} \cdot \bar{z} + \bar{w}x\bar{y}z + \bar{w}xyz + wx \cdot \bar{y} \cdot z + w \cdot \bar{x} \cdot yz + wxyz$$

(d) Implement the circuit of the reduced expression in (c) above using NAND gates only. [6]

(e) Explain how quantifier negation can be used to eliminate the two quantifiers in an expression. Use examples in your explanation. [5]