UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

MAIN EXAMINATION 2005

Title of the Paper: **ELECTRONICS II**

Course Number: **E440 PAPER 1**

Time Allowed: **Three Hours**.

Instructions:

1. Answer any five questions in the following pages.
2. Each question carriers 20 points.

THIS PAPER HAS 7 PAGES, INCLUDING THIS PAGE

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Q1a 10pts: Transform the following Boolean function into:
(1). K-map and
(2) truth table: use hexadecimal number instead of binary code in the table; for example, 12_{hex} instead of 10010_{bin}.
(hint: expand this function into canonical form first)
$F = BE + \overline{B}D\overline{E}$.

Q1b 10pts: Using the tabulation method, simplify the following Boolean function F into either sum of products or product of sums, (not both):
F(v, w, x, y, z)= Σ(2, 6, 9, D, 12, 16, 19, 1B, 1D, 1F)
(hex number in the brackets of the above function)

Q2a 10pts: With the help of K-map, obtain the simplified expressions in (1) SOP and (2) POS of the one of the following two Boolean Functions: (you are allowed to choose only one function and obtain the two expressions of the one you picked)

$G = \overline{A}\overline{B}\overline{C} + A\overline{B}D + \overline{A}\overline{B}C\overline{D} + A\overline{B}\overline{D} + ABC$

$F = (\overline{A} + \overline{B} + D)(A + B + \overline{D})(A + \overline{B} + C + D)(\overline{A} + \overline{D})$

Q2b 10pts: Implement the Boolean function below with only NAND gates and nothing but NAND gates, yet complement inputs are available only at input terminals nowhere else. The implementation must have its function support.

$F = (A + \overline{B})(CD + E)$

Q3a 10pts: Consider a 4-bit register A with bit A_4 being in the most signify-cant position. What is the operation specified by the following state-ments: Show the hardware implementation of the system using a coun-ter with parallel load.

$\overline{A_4}C : A \leftarrow A+1$

$A_4 : A \leftarrow 0$

Function table for a suggested counter register:

Clr	Clk	Load	Count	Function
0	x	x	x	Clear to 0
1	x	0	0	No change
1	↑	1	x	Load inputs
1	↑	0	1	Up Counting

Q3b 10pts: Implement the following function with a multiplexer of 2 bits select address (must have this component) and other elementary gates (possibly an XNOR).

$F(A, B, C, D)= \Sigma(0, 1, 3, 5, 8, 9, F)$

(hex number in the brackets of the above function)

Q4 20pts: Suppose two 2-bit numbers, B_1B_0 and A_1A_0, are to be compared. The comparator will have three outputs: "B=A", "B>A", and "B<A". Assume that B and A are unsigned binary integers. Design a circuit to fit in a PLA. (hint, put the truth table directly into the K-map.)

Q5 20pts: A sequential circuit is described by the following state equations; it has 3 ff's, A, B, and C, and 1 input, x. Design the sequential circuit. Use RS flip-flops to obtain a logic circuit, a state table, a state diagram, and ff input functions. (hint: $Q(t+1)=S+\overline{R}Q(t)$, missing term may be re-placed by $0*Q(t)$)

$A(t+1) = x\overline{B} + AB$

$B(t+1) = xA\overline{B}C$

$C(t+1) = \overline{x}B + \overline{A}B + BC$

Q6 20pts Design a sequential machine, with no restriction on the use of any logic components. Its ASM diagram is shown below. Obtain a state transition table and a circuit diagram plus the support of the logic equations. Two D-ff's are proper to use.

ASM diagram