UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

MAIN EXAMINATION 2005

Title of the Paper: **ELECTRONICS II**

Course Number: **E440 PAPER 2,** Practical Examination

Time Allowed: **Three Hours**.

Instructions:
Points for different sections are shown in the right hand margin.

Special Requirement:
One floppy disc (labeled with your I.D. and name), **which must be handed in, together with your answer sheet,** at the end of the examination

THIS PAPER HAS 3 PAGES, INCLUDING THIS PAGE

DO NOT OPEN THE PAPER
UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

A Data Processor

System Description:

A digital processor has 3 registers, AR, BR, and PR, a parallel full adder, 2 flip-flops for start and stop of the system operation, and additional 2 flip-flops for sequencing the micro-operations. The numbers M and N, involved in the system are both positive non-zero integer only. The start of the system is enabled by manually setting the S-ff H and the stop of the system is by detecting BR=0 or the H of E-ff set by the system. The sequence of the processor operations is described by the following register-transfer operations:

T_0: if (S=H) goto T_1 else goto T_0
T_1: S←L, E←L; PR←0, AR←M, BR←N
T_2: PR←PR+AR, BR←BR-1.
T_3: if (BR=0) then E←H: goto T_0 else goto T_2.

Design Details:

1. Answer what the function of this processor is. **10pts**

The processor basically has two parts: execution and sequencer.

2. The execution part:
   Give the following items:
   A flow chart or an ASM chart, **15pts**
   System circuit diagram; this will be the one shown in the simulation file. **15pts**
3. The sequencer part:
   Implementation may be in the form of a ROM, a PLA, or traditional logic gates (simpler). If a ROM or a PLA, a table of the address and its content is required instead of flip-flop functions
   Give the following items:
   Sequencer circuit diagram: given here, not to be shown in the simulation file. **15pts**
   State diagram **10pts**
   State table **10pts**
   Flip-flop input functions (D-ff is simpler) **10pts**

Simulation:

Simulation itself. **15pts**

Notes for simulation:

a. Set M and N a 4-bit binary number, no sign bit.

b. Because of limited time, simulation covers only the execution part. Thus, manually start the simulation, manually do T_1 and $T_{2,}$, and manually observe BR=0 to stop.

c. Because of limited time and availability of data book, the choice of components is out of the test, so that the following IC's are recommended to use, together with their operation data.

74193 BOR, CAR: -(not used) CUP: -H (not used) CDN: decrmnt, ↑ positive edge Load: -L, load; H, operation	74194 SL, SR: -L (not used) S1, S0: -H parallel mode Clk: to load, ↑ positive edge
74198 SL, SR: -L (not used) S1, S0: -H parallel mode Clk: to load, ↑ positive edge	74283 C4: carry out C0: carry in

d. The use of cable instead of single wire will simplify the circuit wiring. Clear on H or L is a part of this test, so not shown on the data above.