UNIVERSITY OF SWAZILAND

MAIN EXAMINATION 2005/2006

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRONIC ENGINEERING

TITLE OF PAPER: ELECTRONIC SYSTEM DESIGN

COURSE CODE: E330

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer Question ONE and any other THREE questions.
2. Question one carries 40 marks while the other questions each carry 20 marks.
3. If you think not enough data has been given in any question you may assume any reasonable values.

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THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION 1 (COMPULSORY) ***(40 marks)***

Answer all parts of this* question. *Only short answers are expected.

(a) A voltage amplifier has a gain 20 dB, output impedance 2 Ω and maximum current capability of 2 A (signal clips if current increases beyond this. The amplifier output clips when a voltage exceeding 4 V is applied to its input. What is the smallest value of load resistor that can be driven by this amplifier? *(4 marks)*

(b) A 6 V d.c. voltage is connected in series with a switch, a 2 kΩ resistor and a 20 nF capacitor. If we close the switch at $t = 0$ sec, how long will it take for the capacitor voltage to reach 4 V? *(4 marks)*

(c) **(i)** One of two identical resistors is supplied with a d.c. current of 0.5 A. The other is supplied with an a.c. current. After some time the resistors reach the same temperature. What is the peak amplitude of the a.c. current? *(2 marks)*

(ii) An 8.2 Ω load is connected to a 6 V d.c. supply. The power supply input draws 33 mA r.m.s from the 220 V r.m.s, 50 Hz mains. What is the efficiency of the power supply. *(2 marks)*

(d) What is the "equivalent series resistance of a capacitor and why is it an important parameter in selection of capacitors? *(4 marks)*

(e) **(i)** A resistive voltage divider consists of a 10 kΩ ±1% resistor and a 100 kΩ ± 1 % resistor. The voltage divider is used to derive a voltage V_o from a 10 V power supply. What is the possible range of values of the voltage V_o?

(2 marks)

(ii) A 22-kΩ wire-wound potentiometer has 200 turns. What is the output voltage resolution when this potentiometer is used for obtaining a variable voltage from a 10 V d.c. supply? *(2 marks)*

Question 1 continued

(f) Show how you would represent each of the following switches in a circuit diagram:

(i) SPST (momentary). *(1 mark)*

(ii) SPST (maintained). *(1 mark)*

(iii) SPDT (maintained). *(1 mark)*

(iv) SPDT (centre off). *(1 mark)*

(v) DPDT (maintained) *(1 mark)*

(g) Compare double-sided and multilayer boards as far as cost, size and noise immunity are concerned. *(3 marks)*

(h) State a reason for each of the following practices in electronic equipment design and fabrication:

(i) Keying of connectors. *(1 mark)*

(ii) Crimping of flat cable connectors. *(1 mark)*

(iii) Use of ZIF connectors. *(1 mark)*

(iv) Use of isolation transformers. *(1 mark)*

(v) Connection of diodes in parallel with relay coils. *(2 marks)*

(vi) Connection of circuits using opto-isolators. *(1 mark)*

(vii) Use of SMT devices instead of hole mounted devices. *(1 mark)*

(viii) Connection of capacitors between Vcc and ground. *(2 marks)*

(ix) Enclosure of some circuit modules in a metal box. *(1 mark)*

(x) Use of high Q inductors in some parts of a circuit. *(1 mark)*

QUESTION TWO ***(20 marks)***

(a) Explain the meaning of each of the following terms as used in the description of electronic systems:

(i) Reliability

(ii) Failure rate

(iii) MTBF

(iv) Maintainability

(v) MTTF

(5 marks)

(b) The following is an equation used when discussing the failures of items

$$\lambda(t) = \frac{1}{N - n(t)} \frac{dn(t)}{dt}$$

What does each of the terms represent?

(4 marks)

(c) An electronic module has a reliability R. Show that if N such modules are connected in *parallel*, the reliability of the parallel combination is given by $1-(1-R)^N$

(4 marks)

(d) Calculate the 10,000 hr reliability of a radio transmitter which has a failure rate of 5% per 1,000 hr. Find the reliability that would result from operating four such transmitters in parallel for 10,000 hrs, assuming that at least one must be operational for the combination to be effective. *(7 marks)*

QUESTION THREE ***(20 marks)***

A pre-emphasis circuit and its desired response are given in Fig. Q.3. It is required that the input resistance be 50 kΩ and the break frequencies be:

f_1 = 1 kHz and f_2 = 3 kHz.

(a) Write down expressions for:

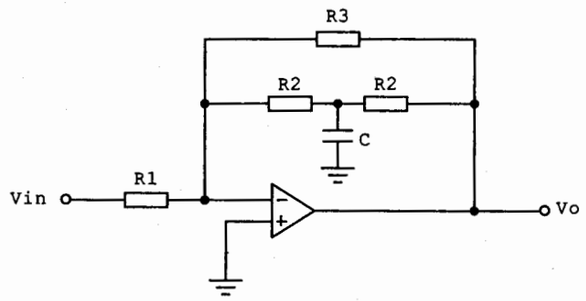
(i) The transfer function in terms of f_1 and f_2 that would realize the required characteristic. *(2 marks)*

(ii) The low frequency gain of the circuit. *(1 mark)*

(iii) The high frequency gain of the circuit. *(1 mark)*

(b) Design the circuit, specifying the values of all the components including the capacitor C. *(12 marks)*

(c) Find the value of a capacitor which could be used in parallel with R3 to make the upper cutoff frequency 50 kHz. *(4 marks)*



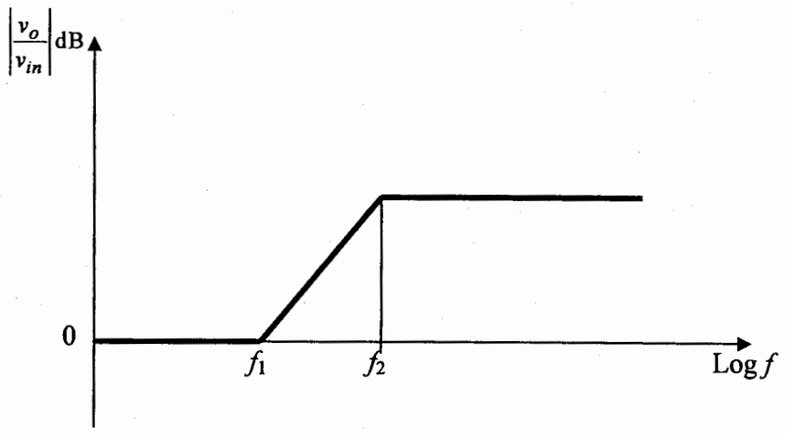


Fig. Q3

QUESTION FOUR ***(20 marks)***

You are a design engineer in a company that wants to develop a portable CD player. Discuss the factors you would take into consideration when developing a design for this product.

QUESTION FIVE ***(20 marks)***

(a) Three amplifiers A1, A2, and A3 of voltage gains 10, 20, and 30 respectively are connected in cascade. The peak output voltages (before clipping) of the amplifiers are ±10 V, ±30 V and ±20 V respectively. Assume no loading effects exist.

(i) What is the maximum input voltage v_{in} and output voltage v_o before clipping occurs? *(2 marks)*

(ii) If the last amplifier has a maximum load current of ±10 mA and it has a load R_L, re-evaluate v_{in} and v_o before clipping occurs. *(2 marks)*

(iii) If the amplifiers are current-limited to ±30 mA. ±20 mA and ±10 mA respectively and voltage clipping occurs at the voltages given above, determine how you would arrange the amplifiers so that you get maximum v_{in} and v_o ? *(4 marks)*

(b) An amplifier comprises two voltage amplifying stages in cascade. The first stage has input resistance, output resistance and voltage gain of 100 kΩ, 1 kΩ and +50 respectively. The same parameters for the second stage are 200 kΩ, 100 Ω and –60 respectively. The amplifier supplies power to a load 10 kΩ with a small stray capacitance C_2 across it. The applied signal is from a 2 mV generator with an internal resistance of 20 kΩ.

(i) Calculate the voltage appearing at the load when capacitive effects are negligible. *(4 marks)*

(ii) Calculate the maximum permitted value of C_2 for the bandwidth of the amplifier to extend up to 5 MHz. *(3 marks)*

(iii) The order of cascading the two stages is changed. Calculate the output voltage appearing at the load when capacitive effects are negligible. *(4 marks)*

(iv) Compare your answer to (i) and (iii) and explain any discrepancy. *(1 mark)*

END. There are no more questions in this paper