UNIVERSITY OF SWAZILAND
FACULTY OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

MAIN EXAMINATION MAY 2006

TITLE OF PAPER: **ELECTRONICS I** **(Paper I)**

COURSE NUMBER: **E360**

TIME ALLOWED: THREE HOURS

INSTRUCTIONS: ANSWER **QUESTION 1** AND ANY OTHER **THREE QUESTIONS**

QUESTION 1 CARRIES 40 MARKS

QUESTION 2, 3, 4, AND 5 CARRY 20 MARKS EACH.

MARKS FOR DIFFERENT SECTIONS ARE SHOWN IN THE RIGHT-HAND MARGIN

THIS PAPER HAS 8 PAGES, INCLUDING THIS PAGE

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Question 1

a) For the circuit shown in Figure 1.A,

(i)If $\beta = 120$, $V_{BEQ} = 0.67V$, $V_{CC} = V_{EE} = 12V$ determine the following I_{BQ}, I_{CQ}, V_{CEQ}.

(ii) Draw the small signal equivalent circuit suitable for use at all possible frequencies.

(iii)Draw the small signal equivalent circuit at mid-band frequencies. [19 marks]

b) In the circuit shown in Figure 1. B, Q_1 and Q_2 are identical transistors having $r_{ds} = 20K\Omega$ and $g_m = 0.2$ siemens.

(i) Which amplifier type does this circuit approximate?

(ii) determine the input and output impedance and the transfer ratio [12 marks]

c) For the oscillator circuit shown in Figure 1.C derive the expression for the return ratio T in terms of A_v. [9 marks]

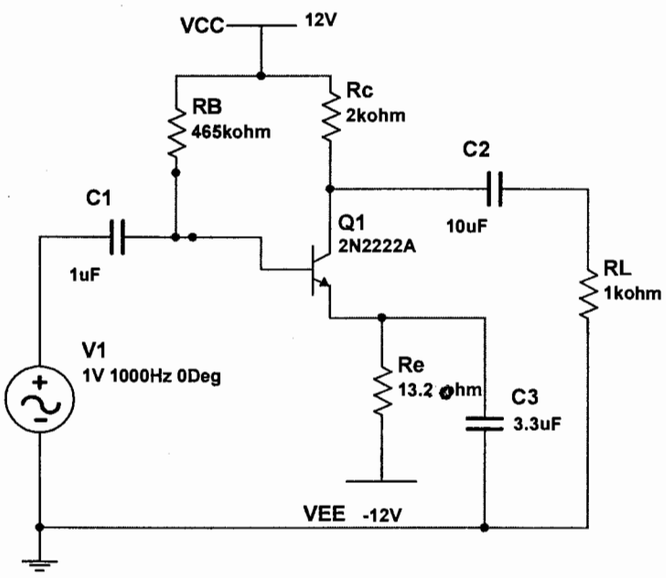

Figure 1. A

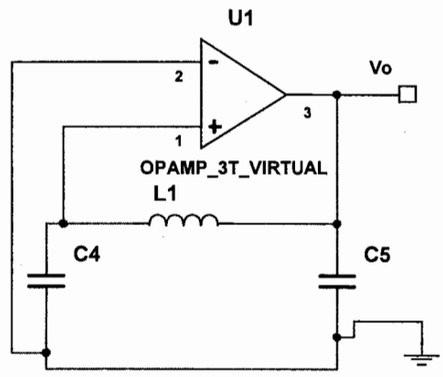

Figure 1 . C

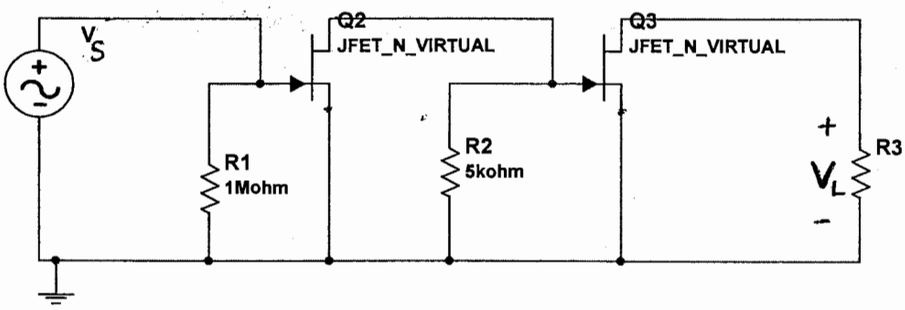

Figure 1. B

Question 2

All diodes in Figure 2 are identical with $V_\gamma = 0.5$ V and the transistor Q1 has a $\beta = 100$ and $V_{BEQ} = 0.63$V when forward biassed..

a) Find V_o for possible combinations of the inputs. [10 marks]

b) Draw a truth table [3 marks]

c) What type of gate is this and write the equation for V_o. [2 marks]

d)In designing ICs it is possible for the design to consist of exclusively MOSFETs and no other components. This is not possible with BJTs Why? [5 marks]

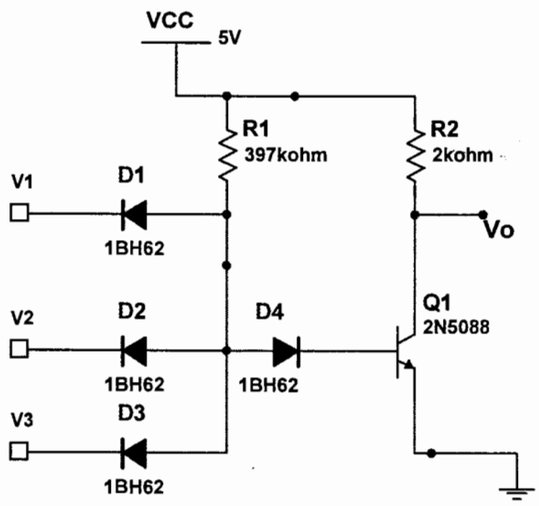

Figure 2

Question 3

Design a single stage common emitter amplifier with self bias and a single 12 volts dc supply, biassing the base through a resistor R_B. The amplifier's voltage gain at mid band frequencies should be -126.4, when connected to a source with internal impedance of a load resistor. The input impedance seen by the source should be equal to 4.5KΩ and the output impedance seen by the load should be equal to 1.145KΩ . The impedance of the source is 100Ω. A *BC 107 transistor* biassed at V_{CEQ} = 5volts and I_{CQ} = 5.128 mA with β = 120 should be used. The other parameters for this transistor are g_m = 0.2051 siemens, r_π = 5 KΩ and r_o = 25KΩ.
[Hint: find values of R_B, R_C, R_L, and R_E] [20 marks]

Question 4

a) Derive the expression for the output voltage V_o in terms of voltages (x, y, z) and the resistors as shown in Figure 4. [8 marks]

b) Explain how the circuit in Figure 4 works? [6 marks]

c)What would be the theoretical range for the input voltages (x, y, z) and the output, and what would limit the values of the input voltages? [6marks]

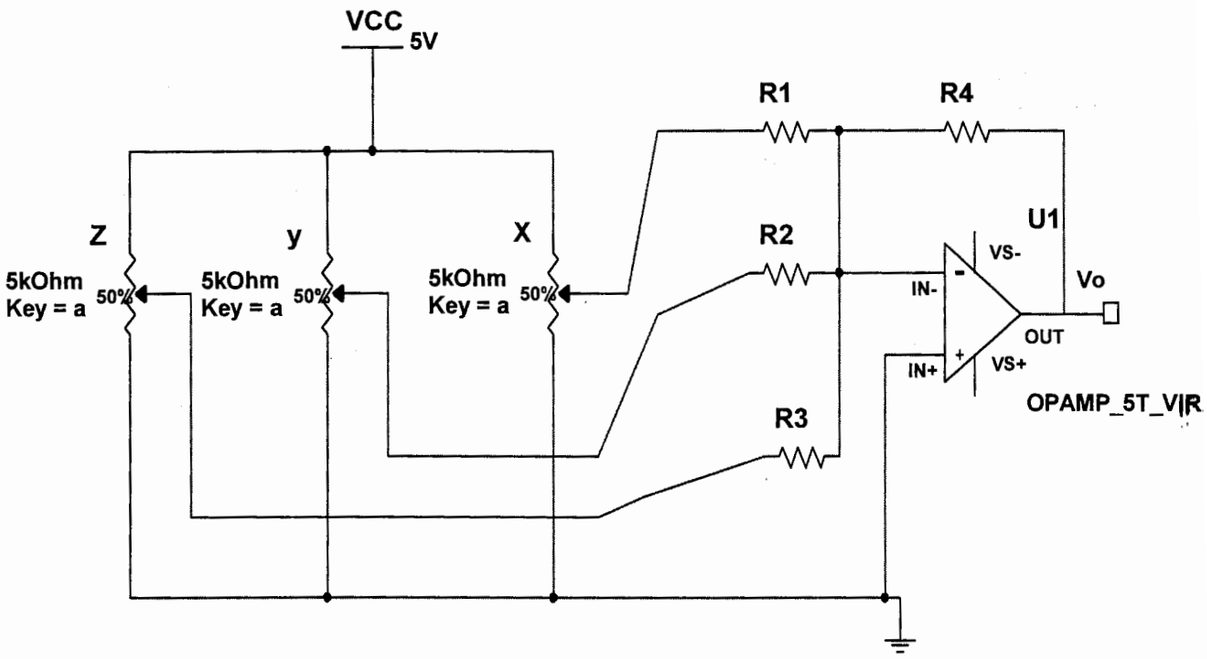

Figure 4 **|Vs|=12volts**

Question 5

For the power amplifier shown in figure 5 calculate

(a) the power dissipated by the circuit when v_i is zero. [5 marks]

(b) the maximum and minimum collector current [11 marks]

(c) the power available at the output Vo [4 marks]

Note: $\beta = 16$, $V_{BE} = 0.7$ and $V_1 = 2\sin(\omega t)$

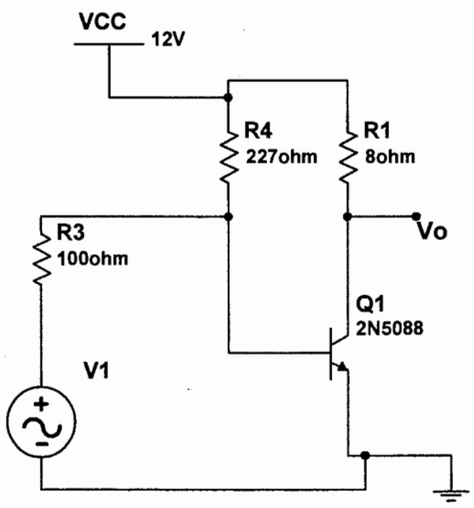

Figure 5