UNIVERSITY OF SWAZILAND

MAIN EXAMINATION 2005/2006

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRONIC ENGINEERING

TITLE OF PAPER: ELECTRONICS III—PAPER 1

COURSE NUMBER: E510

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. **Answer any <u>FOUR</u> (4) of the following six questions.**
2. **Each question carries 25 marks.**
3. **Unless otherwise stated, $V_{BE(ON)} = 0.7$ V and $V_T = 0.026$ V.**
4. **If you think not enough data has been given in any question you may assume reasonable values.**
5. **In design, when necessary, use the following E24 range of values:**

   10 11 12 13 15 16 18 20 22 24 27 30 33 36 39 43

   47 51 56 62 68 75 82 91

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THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION 1

(a) Find the voltages V1 and V2, and the currents I1, I2, and I3 in the circuit of Fig. 1. Assume |VBE| = 0.7 V for all transistors and $\beta = \infty$.

[10 marks]

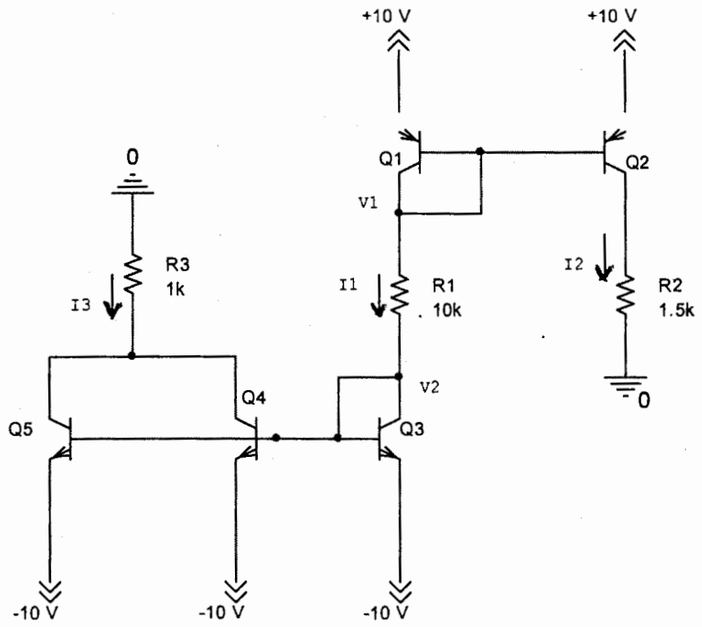

Fig. Q1a

(b) The differential amplifier of Fig. Q1b utilizes a resistor connected to the negative power supply to establish the bias current I. Assume $V_{BE} = 0.7$ V and $V_A = 50$ V.

(i) For $v_{B1} = v_{id}/2$ and $v_{B2} = -v_{id}/2$, where $v_{id}/2$ is a small signal with zero average, find the magnitude of the differential gain, $|v_o/v_{id}|$.

(ii) For $v_{B1} = v_{B2} = v_{icm}$, find the magnitude of the common-mode gain, $|v_o/v_{icm}|$.

(iii) Calculate the CMRR in dB.

[15 marks]

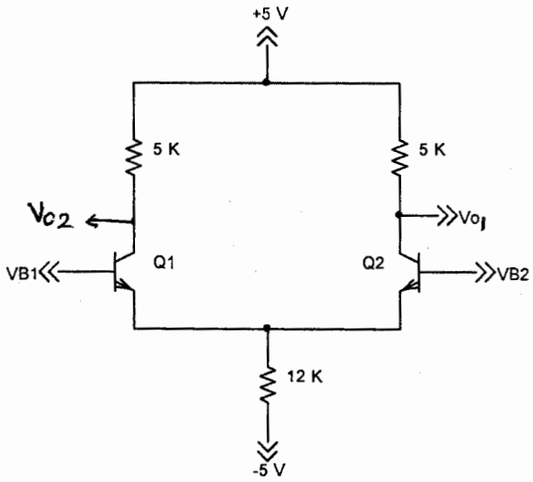

Fig. Q1b

QUESTION 2

Fig. 2 shows a circuit for a differential amplifier with active load. Here Q_1 and Q_2 form the differential pair while the current source transistors Q_4 and Q_5 form the active loads for Q_1 and Q_2, respectively. The dc bias circuit that establishes an appropriate dc voltage at the drains of Q_1 and Q_2 is not shown. It is required to design the circuit to meet the following specifications:

- Differential gain $A_d = 100$V/V.
- $I_{REF} = I = 200$ μA.
- The dc voltage at the gates of Q_6 and Q_3 is +1.3 V.
- The dc voltage at the gates of Q_7, Q_4 and Q_5 is +1.3 V.

The technology available is specified as follows: $k'_n = 3k'_p = 120$ μA/V; $|V_{tn}| = |V_{tp}| = 0.5$ V; $|V_{An}| = |V_{Ap}| = 20$ V.

(a) Specify the required value of R.

(b) Specify W/L ratio, $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_6$ for transistors Q_3 and Q_6.

(c) Specify W/L ratio, $\left(\frac{W}{L}\right)_7$ for transistor Q_7.

(d) Specify W/L ratio, $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$ for transistors Q_1 and Q_2.

(e) Specify W/L ratio, $\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5$ for transistors Q_4 and Q_5.

For dc bias calculations you may neglect channel-length modulation. You may find the following formulae useful:

$$g_m = \frac{I}{V_{OV}} = \frac{I}{V_{GS} - V_t} \qquad r_o = \frac{V_A}{I_D} \qquad I_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right)(V_{OV})^2$$

[25 marks]

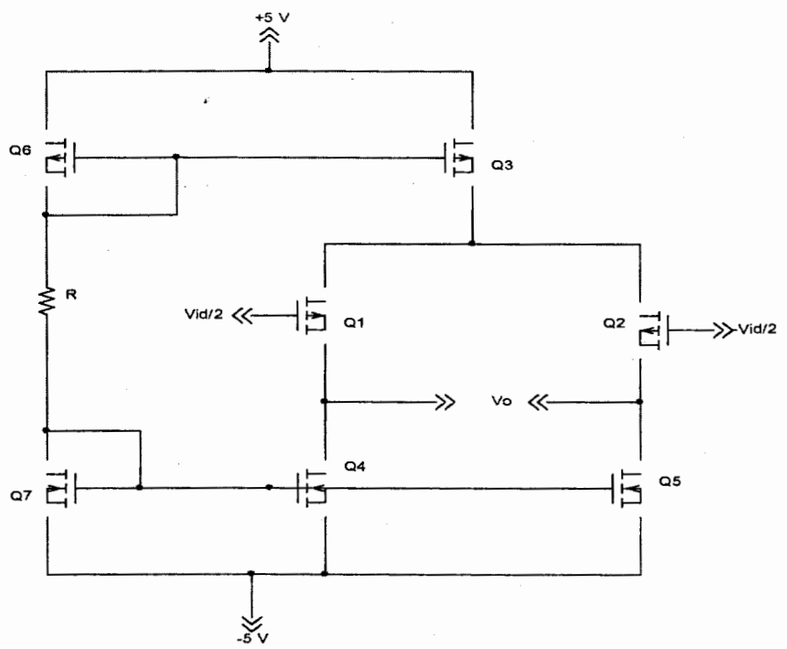

Fig. 2

QUESTION 3

Fig. 3 shows a class AB output stage with short-circuit protection. The output stage is meant to supply a maximum average power of 3.125 W to a 16-Ω speaker. The output transistors Q_1 and Q_2 both have minimum value of $\beta = 50$.

(a) If a current of 2 mA must flow through the V_{BE} multiplier circuit when Q_1 is supplying the peak load current, determine suitable value for I_{bias}.

[9 marks]

(b) Select suitable values for R_1 and R_2 so that the V_{BE} multiplier will provide $V_{BB} = 1$ V for biasing the output transistors. Since minimum current through the V_{BE} multiplier is 2 mA, assume that current through R_1 and R_2 is 1 mA. Use $V_{BE3} = 0.6$ V.

[8 marks]

(c) Select suitable value for $R_{e1} = R_{e2}$ for short-circuit protection such that Q_4 turns on and absorbs all of I_{bias} when the load current reaches 1.5 A. For Q_4, $I_s = 10^{-14}$ A.

[8 marks]

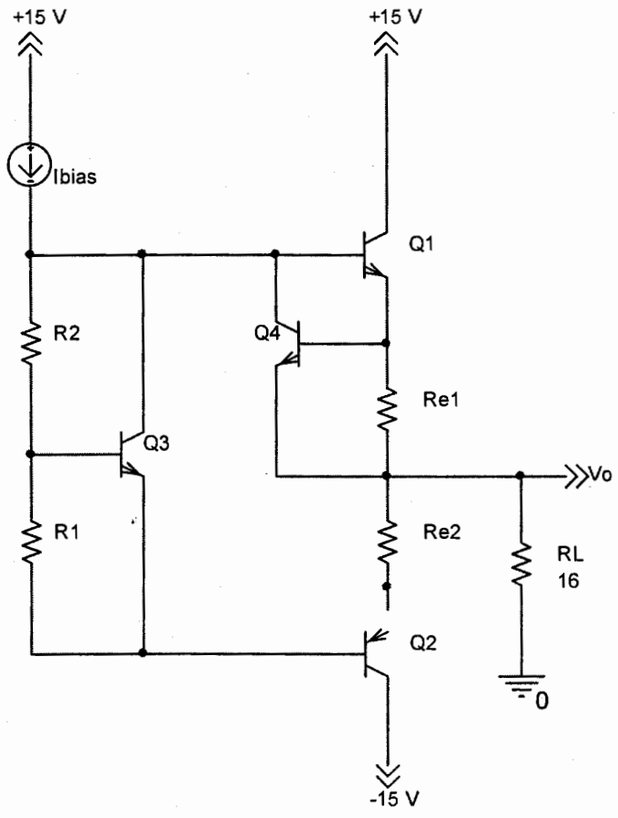

Fig. 3

QUESTION 4

An IF amplifier for an AM radio receiver is to be designed with f_o = 455 KHz and a 3-dB bandwidth of 10 KHz.

(a) Using two stagger-tuned stages, find f_{o1}, B_1, f_{o2} and B_2.

[11 marks]

(b) Using 500 μH inductors, find C and R for each stage.

[14 marks]

QUESTION 5

(a) In the current differencing amplifier of Fig. Q5a, v_i = 100 mV. Calculate A_v and $V_{o(AC)}$.

[10 marks]

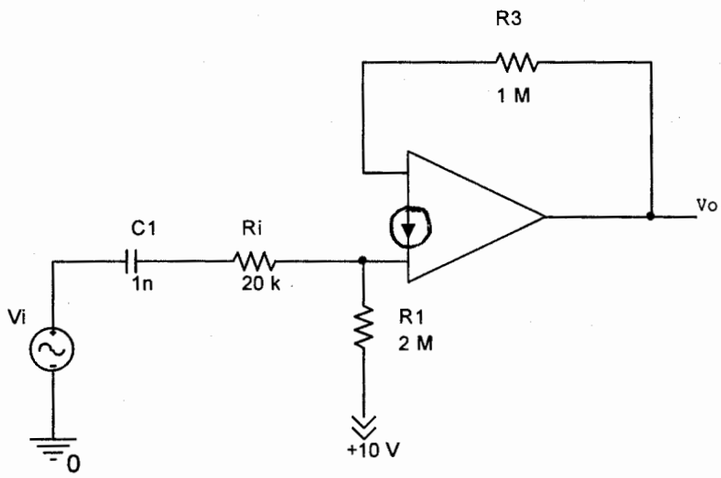

Fig. Q5a

(b) Given a CA3080 operational transconductance amplifier (OTA) with a supply voltage ±V = ±10 V and an I_{ABC} of 100 μA, find: (i) the OTA transconductance g_m; (ii) the output voltage with an input of 10 mV and a load resistor of 1 KΩ; (iii) the I_{ABC} needed to give a I V output with a 120 mV input and a load resistance of 1 KΩ.

For the CA3080 OTA,

$$g_m = \left(\frac{300}{V}\right)(I_{ABC})$$

[15 marks]

QUESTION 6

A PLL is needed with a capture range (f_c) of 200 Hz, and a free running frequency (f_o) of 10 KHz. The NE565 PLL IC is to be used. ±5 V supplies are connected to the NE565, so that $V_{net} = 10$.

(a) Determine the lock range (f_L).

[5 marks]

(b) Choose component values, R_1, C_1, and C_2, which when connected to the NE565 will give these parameters.

[15 marks]

(c) How would you reduce the lock range to 4000 Hz?

[5 marks]

For the NE565 PLL:

$$f_o = \frac{1}{3.7 R_1 C_1}$$

$$f_L = \pm \frac{8 f_o}{V_{net}}$$

$$f_c = \pm \sqrt{\frac{f_L}{2\pi(3600)(C_2)}}.$$