UNIVERSITY OF SWAZILAND
FACULTY OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

MAIN EXAMINATION 2007

TITLE OF PAPER : INTRODUCTION TO ANALOG & DIGITAL ELECTRONICS

COURSE NUMBER : E212

TIME ALLOWED : THREE (3) HOURS

INSTRUCTIONS : ANSWER ANY FOUR OUT OF THE FIVE QUESTIONS

EACH QUESTION CARRIES 25 MARKS

MARKS FOR DIFFERENT SECTIONS ARE SHOWN IN THE RIGHT-HAND MARGIN

THIS PAPER HAS 6 PAGES, INCLUDING THIS PAGE

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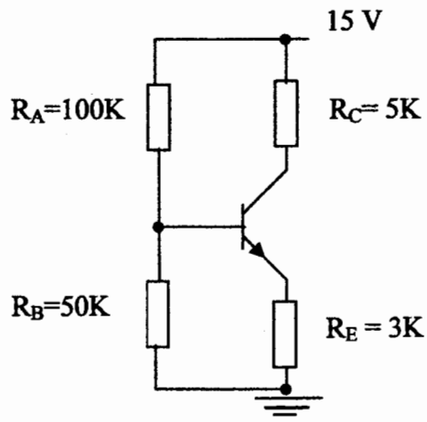
Question 1

(a) Given that $I_C = \alpha I_E$ and $I_C = \beta I_B$, where α and β are constants. Derive an expression relating α and β (4 marks)

(b) Given the following figure, determine all node voltages and branch currents. Assume that the transistor has $\beta = 100$ and $V_{BE}=0.7V$, and negligible reverse saturation current (10 marks)



(c) Design a base bias circuit for a transistor with an average $\beta=60$, using a 10 V power supply. The design should be for an initial collector current I_C =10 mA. Assume $V_{BE}=0.7V$

(7 marks)

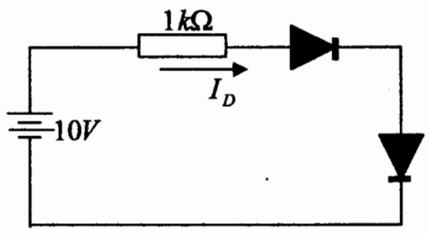
(d) With the aid of a common-emitter BJT circuit, explain how a BJT operates as a switch (4 marks)

Question 2

(a) With the help of appropriate diagrams, describe forward and reverse biasing of a silicon diode (6 marks)

(b) A semiconductor diode, the forward and reverse characteristics of which can be considered ideal, is used in a half-wave rectifier circuit supplying a resistive load of 1000 Ω. If the r.m.s. value of the sinusoidal supply voltage is 250 V, determine the peak diode current and the r.m.s. diode current (3 marks)

(c) Find the diode current in the circuit shown below (3 marks)



(d) A bridge rectifier is driven by a 60 Hz sinusoid with root mean square (RMS) voltage of 70.711 V. The load resistance R_L = 10 kΩ and the smoothing capacitor is C= 83.3 μF. Calculate the output ripple voltage. What is the purpose of the smoothing capacitor in the rectifier?

(4 marks)

(e) With the help of a well-labelled diagram, discuss the operation of an n-channel enhancement type MOSFET

(6 marks)

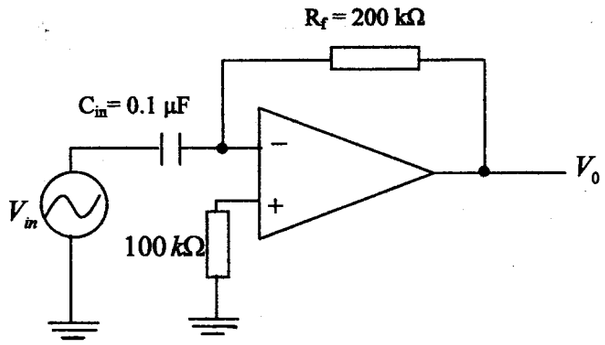
(f) State the three regions of operation of a MOSFET and give the conditions for the FET to be in each of the three regions in terms of V_{GS}, V_t and V_{DS}

(3 marks)

Question 3

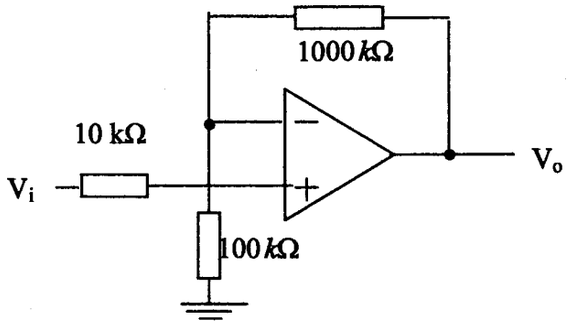
(a) Give any four characteristics of an ideal operational amplifier (4 marks)

(b) Calculate V_0 as a function of time for the circuit shown below given that $V_{in} = A\sin(\omega t)$, where A=500 mV and ω = 100 rad/s (4 marks)



(c) An operational amplifier has an open loop gain of 200 000. The voltage supply is between 15V and -15V. Assuming that output voltage limits of the amplifier are 1.5V below the supply voltage, calculate the voltage swing needed at the inputs to go from negative saturation to positive saturation (5 marks)

(d) State the function of the following amplifier and calculate its gain (2 marks)



(e) Three voltages, 4 V, 3 V and 2 V, are applied to the three input resistors of a summation amplifier which are 10 kΩ , 30 kΩ and 18 kΩ , respectively. What should the feedback resistor be in order to get an output voltage of -34.2 V? (3 marks)

(f) Design a circuit incorporating Op-Amp(s) that produces the following output, where *y* is the input

$$12 - 6\frac{dy}{dt}$$ (5 marks)

(g) Explain *input offset voltage* when used in association with Op-Amps (2 marks)

Question 4

(a) (i) Convert decimal 0.6875 to binary (2 marks)
(ii) Convert the fractional binary 0.1101 to decimal (2 marks)

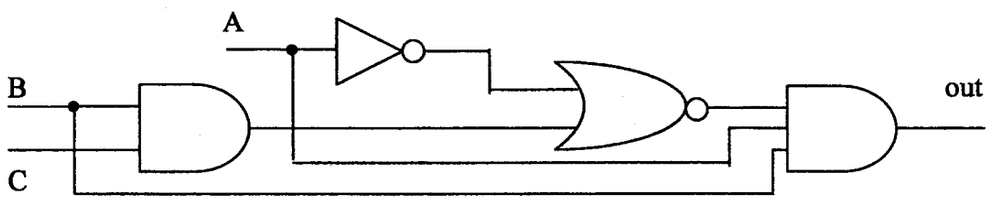
(b) Eliminate the OR operations from the following expressions:

(i) $A + B.\overline{C}$ (2 marks)
(ii) $\overline{A.B} + C + D$ (2 marks)

(c) Using only NAND gates, draw circuit for:

$A.(B + C)$ (4 marks)

(d) (i) Implement the following digital circuit with the fewest number of gates (7 marks)



(ii) Prepare a Truth Table for the following Boolean function (6 marks)

$$F = \overline{X}YZ + \overline{X}Y\overline{Z} + XZ$$

Question 5

(a) Briefly discuss the following method of forming PN junctions

solid state diffusion (5 marks)

(b) Briefly discuss how crystal growth is achieved by using the Crucible grown process (Czochralski (CZ) process)

(8 marks)

(c) Give two advantages and one disadvantage of the Float Zone (FZ) process over the CZ process in crystal growth

(6 marks)

(d) Derive an expression for the output of the circuit shown below (6 marks)