UNIVERSITY OF SWAZILAND
FACULTY OF SCIENCE

DEPARTMENT OF ELECTRONIC ENGINEERING
MAIN EXAMINATION, DECEMBER 2006

TITLE OF PAPER : ANALOGUE ELECTRONICS

COURSE NUMBER : E361

TIME ALLOWED : THREE HOURS

INSTRUCTIONS : READ EACH QUESTION CAREFULLY
ANSWER ANY **FOUR** OUT OF **FIVE** QUESTIONS.
EACH QUESTION CARRIES **25 MARKS.**
MARKS FOR EACH SECTION ARE SHOWN
ON THE RIGHT-HAND MARGIN.

THIS PAPER HAS 8 PAGES INCLUDING THIS PAGE.

THIS PAPER IS NOT TO BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

QUESTION 1

(a) (i) Design a diode circuit to supply 1.5 V to a load resistor. The diode is connected to a 5 V supply through a resistor R, has a specification of a 0.7 V drop at a current of 10 mA and $\eta = 1$. (3 marks)

(ii) Using the constant Voltage drop model, specify the value of R. (5 marks)

(iii) What is the output voltage when the load is disconnected? (2 marks)

(iv) For fixed bias voltage, how will doubling the load affect the voltages across each component in the circuit? (3 marks)

(b) The circuit in Figure 1 shows a MOSFET Q1 having output characteristics displayed on Figure 2 and a load MOSFET Q2 with characteristics displayed on Figure 3.

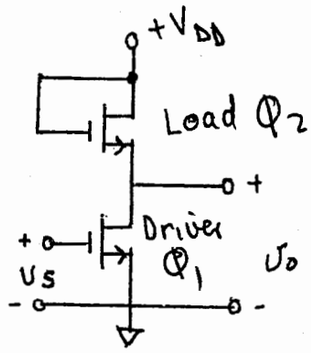

Figure 1

(i) Plot the resistance characteristics of the load MOSFET Q2 onto Figure 3. (8 marks)

(ii) Plot the voltage transfer characteristic $v_o = V_{DS1}$ versus $v_s = V_{GS1}$ for the circuit of Figure 1. (4 marks)

NOTE: IF YOU HAVE ANSWERED THIS QUESTION, REMEMBER TO HAND IN FIGURE 2 AND FIGURE 3 WITH YOUR ANSWER BOOKLET(S). MAKE SURE YOUR EXAM. NO. IS CLEARLY WRITTEN AT THE TOP OF THIS PAGE

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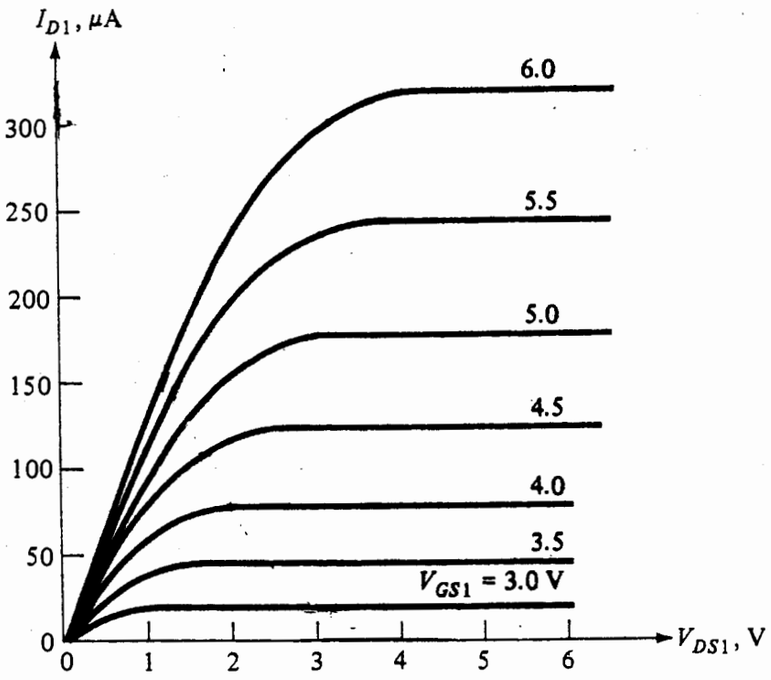
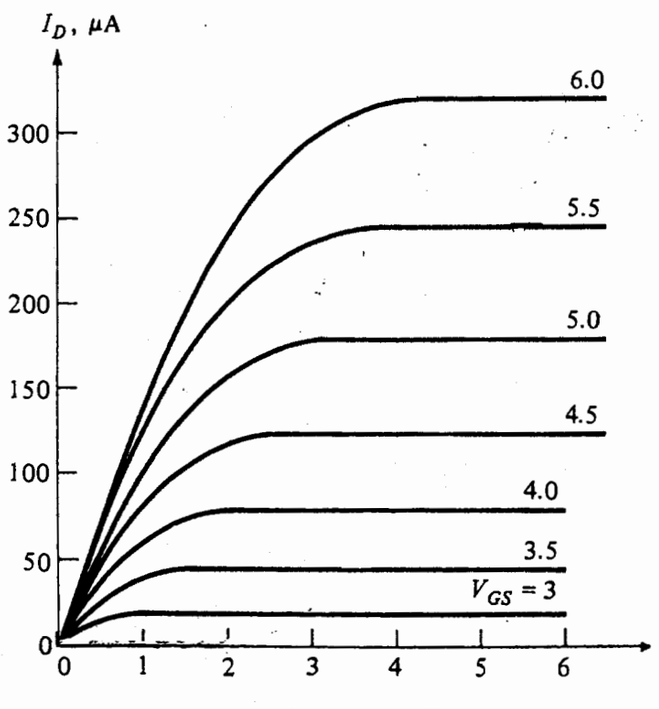


3 marks

Figure 2



3 marks

Figure 3

QUESTION 2

(a) An Operational Amplifier is used in a circuit such that the output is a linear combination of the input signals.

(i) Present the circuit diagram to sum four input signals and derive the corresponding expression of the output signal. (6 marks)

Let the design in (i) be such that $R_1 = R_f = 1\ k\Omega$ and $R_2 = 2R_1$ i.e. $R_n = 2R_{n-1}$. The input voltages $v_1, \ldots v_n$ can be 0 or 10 V. Note that $_{n} = 4$.

(ii) What is the smallest output voltage if at least 1 input is nonzero? (1 mark)

(b) The dc model of the silicon diode in Figure 4 at 20 °C has $V_\gamma = 0.6$ V and $R_f = 0$.

The input signal $v_s = 5 + 0.029 \sin \omega t$ V. Neglecting the effect of the diffusion capacitance,

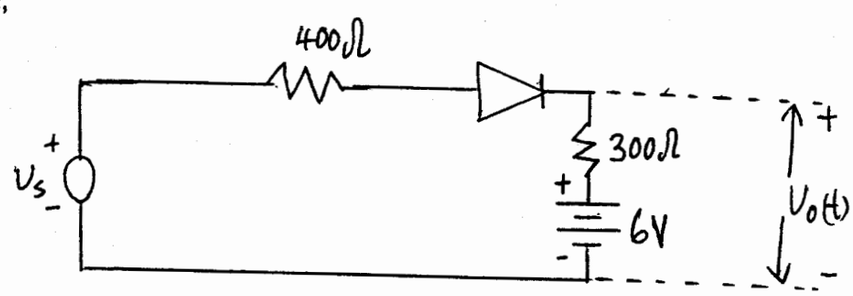


Figure 4

(i) present the large and small signal models of the circuit. (4 marks)

(ii) Determine the instantaneous output voltage . (11 marks)

(iii) Sketch 2 cycles of the output voltage that would appear on an oscilloscope when the selector knob is set to ac. (3 marks)

QUESTION 3

In the design of Figure 5, resistor R_B has been selected to bias the BJT in the forward - active region at a base current $I_B = 40\ \mu A$. The output characteristics are given in Figure 6.
The voltage amplitude of v_s is chosen to provide peak base current $I_{bm} = 15\ \mu A$.

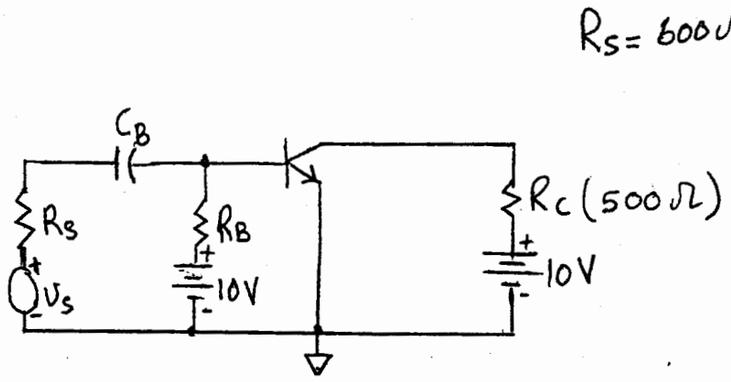


Figure 5

(i) Using the concept of the load line with Figure 6, compute quiescent values of both the collector current and voltage. (7marks)

(ii) Present the low - frequency small signal equivalent of the circuit in Figure 5. The effect of r_o can be considered negligible and r_b taken as $100\ \Omega$.

Assuming operation at room temperature, determine the signal voltage gain. (18 marks)

NOTE: IF YOU HAVE ANSWERED THIS QUESTION, REMEMBER TO HAND IN FIGURE 6 WITH YOUR ANSWER BOOKLET(S). MAKE SURE YOUR EXAM. NO. IS CLEARLY WRITTEN AT THE TOP OF THIS PAGE

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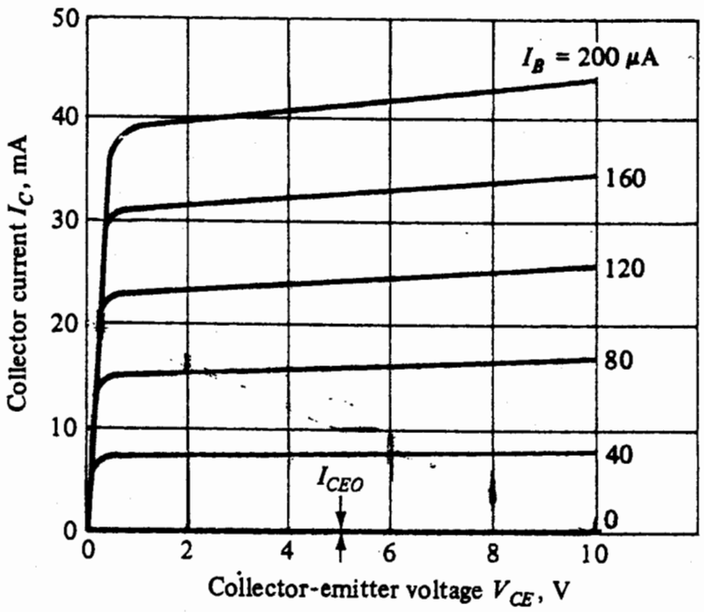

Figure 6

QUESTION 4

(a) Figure 7 shows an Operational Amplifier design circuit with $R_1 = 100\ k\Omega$ and $C_f = 0.1\ \mu F$.

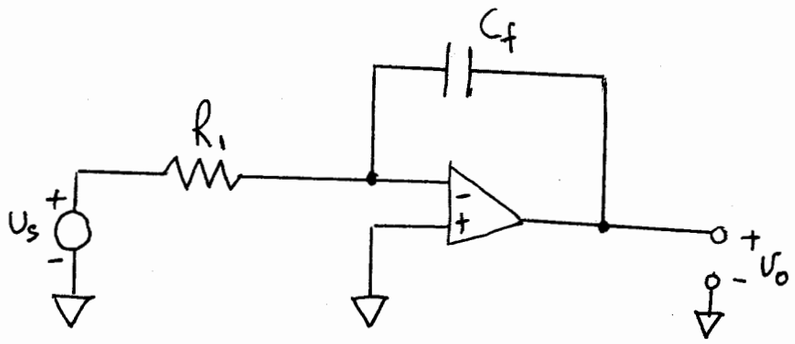

Figure 7

(i) Derive an expression relating v_o and v_s. (4 marks)

(ii) Compute and sketch v_o as a function of time for $v_s = -10$ mV. Assume switching at time $t = 0$. (5 marks)

(iii) Compute and sketch v_o as a function of time for a 5 V - 1 kHz sinusoidal input signal. (6 marks)

(b) The waveform

$$v_s = \begin{cases} -V_1 & \text{for } t < T_1 \\ +V_2 & \text{for } T_1 < t < T_2 \\ -V_1 & \text{for } t = T_2 \end{cases}$$

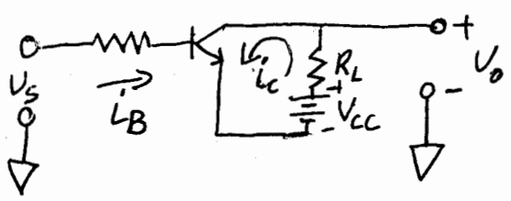

Figure 8

is used as input to the circuit of Figure 8. The value of voltage V_2 ensures operation at the edge of saturation. Neglecting the reverse - current components, sketch the output voltage and current waveforms. (10 marks)

QUESTION 5

(a) The JFET in Figure 9 is biased at I_D = 6 mA and V_{DS} = 10 V, V_p = -6 V, I_{DSS} = 15 mA and λ = 0.02 V^{-1}.

$$r_{ds} = 1 + \lambda V_{DSQ} \frac{1 + \lambda V_{DSQ}}{\lambda I_{DS}}$$

$$g_m = \frac{-2I_{DSS}}{V_p}\left(1 - \frac{V_{GSQ}}{V_p}\right)$$

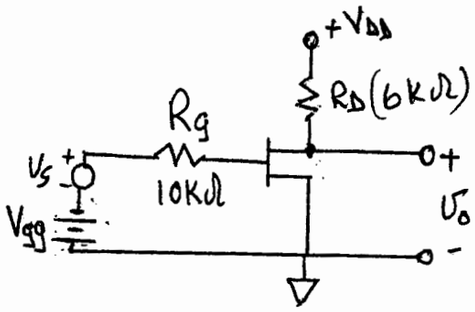

Figure 9

Compute the required value of R_D for the amplitude of the signal component of v_o to be 10 times that of v_s. (13 marks)

(b) Given the following for Figure 10:

$\beta_F = 125$

$\beta_o = 125$

$R_1 = 72k\Omega$

$R_2 = 18k\Omega$

$R_E = 1.4k\Omega$

$R_C = 4.0k\Omega$

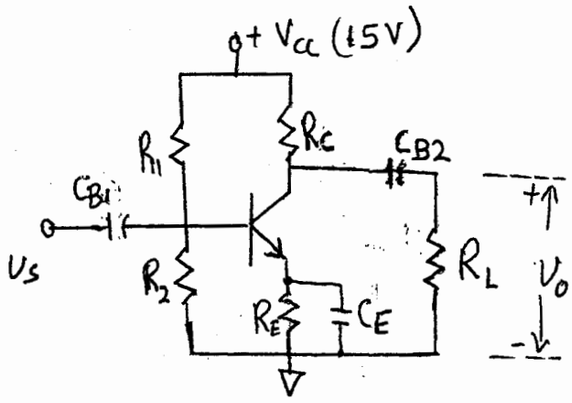

Figure 10

Determine the operating point. (9 marks)

(c) What are the main functions of C_{B1}, C_{B2} and C_E? (3 marks)

The End of Exam. Questions.