UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

July 2007
SUPPLEMENTARY EXAMINATION

Title of the Paper: **DIGITAL ELECTRONICS I**
Course Number: **E362**
Time Allowed: **Three Hours**.

Instructions:
1. To answer, pick any five out of seven questions in the following pages.
2. Each question carriers 20 points.
3. This paper has 8 pages, including this page.

DO NOT OPEN THE PAPER
UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

Q1 20pts: Using the tabulation method, simplify the following Boolean function F into an SOP format.

$F(v, w, x, y, z) = \Sigma(0, 4, C, D, E, F, 10, 11, 12, 14, 15, 16)_{hex}$

(hex number in the brackets of the above function)

Q2a 10pts: Convert the number, 25.37_{dec}, into a binary and a hexadecimal number. If the number of digits after decimal point is infinite, give one cycle if cyclic or else at least 10 digits.

Q2b 10pts: Compute the results of the following arithmetic expressions.
(1) $10.101\text{-}100.1]_{dec}$ (2) $10.01 \bullet 101.1]_{bin}$

Q3a 10pts: With the help of a K-Map (must use K-Map), obtain the simplified expressions of the following Boolean Function in both SOP and POS format:

$$F(A,B,C,D,E) = \overline{B}(A\overline{D} + \overline{E}) + \overline{A}DE$$

Q3b 10pts: Implement the Boolean function below with only NOR gates and nothing but NOR gates, yet complement inputs are available only at input terminals nowhere else. The implement must have its function support.

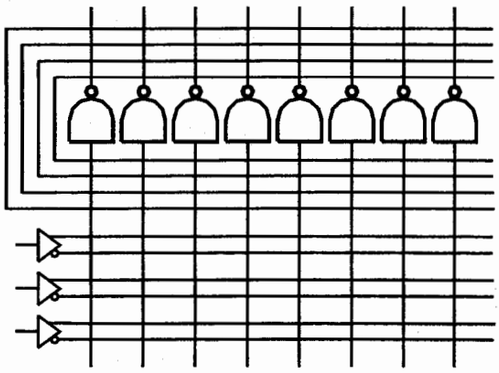
$$C(x,y,z) = xy + yz + xz$$

$$S(x,y,z) = \overline{C}(x + y + z) + xyz$$

Q4a 10pts:

$F(x, y, z)=\Pi(0, 1, 3, 6)$

Implement the above function with a PAL structure. Function support of this implementation is required. Simplification might be needed.

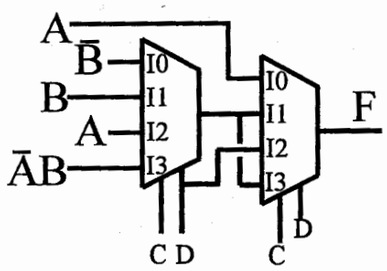


Q4b 10pts: Realize the Boolean function below,

$F(D,C,B,A)=\Sigma(3,4,7,9,B,C,D,F)_{hex}$,

with one 4-1 mux of address DA.

Q5a 10pts: Complete the 4-input K-map for the following Mux circuit.



CD / AB	00	01	11	10
00				
01				
11				
10				

Q5b 10pts: You have two Quad 2-1 Muxs and one 8-1 Mux. Make use of these components to implement a larger Mux. The larger, the better it is. Give the circuit and the address arrangement.

Q6a 10pts: Design a combinational circuit, which will do multiplication of two 2-bit input data with conventional gates. How many bits will the product result be?

Q6b 10pts: Use ROM to implement an addition table of two 3-bit binary numbers A and B. Be aware that the ROM address and the data are both always in Hex number and that the addresses are always continuously numbered. Find the specifications of the ROM (ie, the size of address byte and data byte) and the ROM contents in the ROM memories. How the address and the data are related to the numbers A and B and the sum.

Q7a 16pts: Use logical statements to design a 4-bit magnitude comparator.

Q7b 4pts: Modify the above design (use the above circuit as a block) to check if the two input data, A and B (both of 4-bit), are equal or not. Then, the circuit has only one output x, so that x=1 if A=B, and x=0 if A≠B