# UNIVERSITY OF SWAZILAND

## MAIN EXAMINATION, MAY 2007

## FACULTY OF SCIENCE

## DEPARTMENT OF ELECTRONIC ENGINEERING

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|---|---|
| TITLE OF PAPER: | DIGITAL ELECTRONICS II |
| COURSE CODE: | E442 |
| TIME ALLOWED: | THREE HOURS |

INSTRUCTIONS:

1. There are seven questions in this paper. Answer any FIVE questions.
2. Each question carries a total of 20 points as indicated.

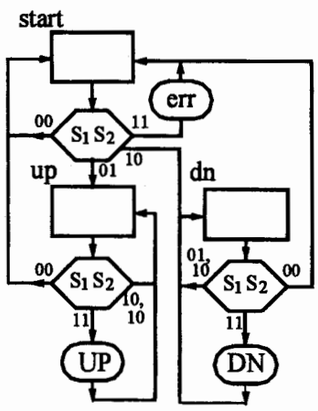
**THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR**

**THIS PAPER CONTAINS EIGHT (8) PAGES INCLUDING THIS PAGE**

ASM Chart:

**Q1a 10pts:** Drive a state table from the given ASM chart on the right.

**Q1b 10pts:** Convert the given ASM chart on the right into a state diagram.



Registers and Counters:

**Q2a 10pts:** Draw a block diagram to show all control signals, data inputs, and data outputs of a universal binary up-down counter.

**Q2b 10pts:** For a universal binary up-down counter, describe, using block diagram, two techniques to change the counting mod to 9.

Register-Transfer Circuit:

**Q3** It is required to exchange data between two registers regA and regB. Use RAM as the intermediate storage device. regA, regB, and RAM are of the same byte size and in a common bus structure.

**(a) 10pts:** Draw the hardware circuit for this system. Of course, MAR, MBR, and memory unit must be included.

**(b) 10pts:** Use registry language to describe the operation.

Practical design with ASM

**Q4 20pts:** Design an ASM chart of the operation process of a vending machine. It is a machine of returning no change and dispenses a can when the user inserts an amount equal or more than E2.50. A coin recognizing interface will input an appropriate code to the system as follows: 00=no coin, 01=50 cents, 10=E1.00, and 11=E2.00. A dispensing output is generated when there is enough money, to dispense a can. You must break the whole operation process into several stages or states. The suggested stages are: "insert coin", "more coin", "no more", and "dispense".

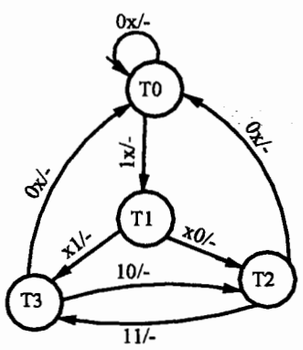
Control Circuit Design

**Q5 20pts:** Shown below is a 4-state state diagram of a control unit where control inputs are xy and output is nothing, as a whole symbolically xy/-. Design the control circuit by the sequence register and decoder structure with two JK ffs $G_2$ and $G_1$.

**(a)** Use the decoder outputs as conditions for the present states.

**(b)** Use the ff outputs as conditions for the present states.

Compare the two results and comment on the advantages and disadvantages in each case.



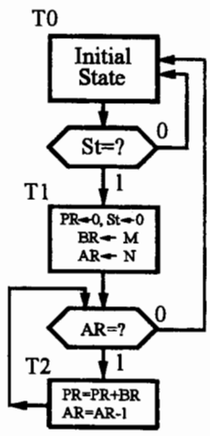
**Q6 20pts:** Shown on the right is the flowchart of a digital system that multiplies two unsigned binary integers (assume 4-bit data) by the repeated addition method.

(a). List the register transfer statements executed in each state,

(b). Draw a state diagram for the control,

(c). Design the control by the one ff per state structure,

(d). Draw the whole circuit of the system in a block diagram form.



Micro-Operation and Simple Computer:
**Q7** An instruction is specified as follows:

| Mnemonic | | Description | Function |
|---|---|---|---|
| ADI | OPRD | Add operand to RegA | A←A+Oprd |

**(a) 10pts:** List the sequence of micro-operations (given in the textbook) for executing this instruction. Note that this operand is located next to the Op-Code in the memory address.

**(b) 10pts:** Design with blocks the circuit required to perform this instruction. This circuit is not meant to be a general computer but a circuit sufficient for this instruction only. All control signal must be included and marked.