UNIVERSITY OF SWAZILAND

MAIN EXAMINATION DECEMBER 2006

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE ELECTRONICS III
COURSE NUMBER:	E511
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. **Answer any <u>FOUR</u> (4) of the following six questions.**
2. **Each question carries 25 marks.**
3. **Unless otherwise stated, $V_{BE(ON)} = 0.7$ V and $V_T = 0.025$ V.**
4. **If you think not enough data has been given in any question you may assume reasonable values.**
5. **A sheet containing some useful equations is attached at the end of the examination paper.**

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS EIGHT (8) PAGES INCLUDING THIS PAGE

QUESTION ONE

(a) A diode has $v_D = 0.7$ V at 1 mA and is characterized by n = 2. It is connected in series with a 150-Ω resistor to a 1.2 V dc supply. Using iterative analysis and the exponential diode model, give an accurate (to 3 significant figures) estimate of the current through the diode. *(10 marks)*

(b) Using basic principles of ideal opamp circuits (such as i_{in} =0) and the diode exponential model obtain the relationships between the output and input voltages in each of the three circuits in Fig. Q1b. Specify the range of validity of the input voltages.

(7 marks)

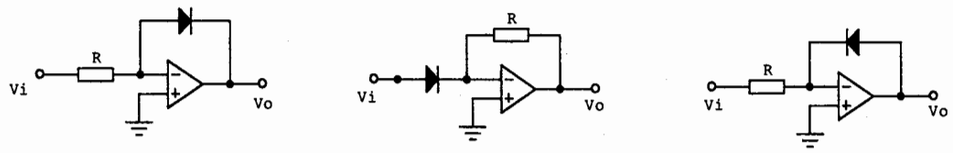

Fig. Q.1b **(i)** **(ii)** **(iii)**

(c) Use the results obtained in (b) to show that the circuit in Fig. Q.1c is a multiplier of the voltages v_1 and v_2. Assume that all diodes are matched and the resistors are equal. Specify the range of validity of these voltages.

(8 marks)

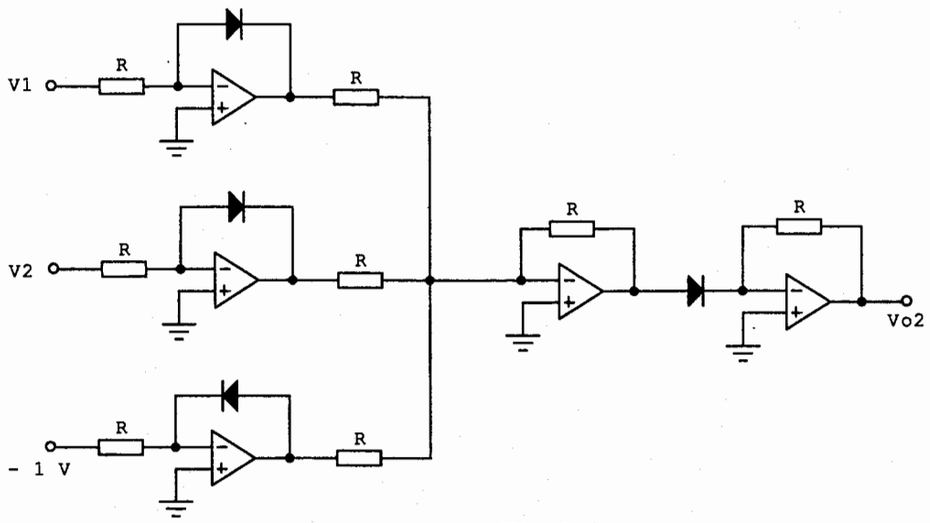

Fig. Q.1c

QUESTION TWO

(a) A circuit designer has produced the current mirror circuit shown in Fig. Q2a. Transistors Q1 and Q2 may be assumed to be matched. On testing the circuit it is found that it does not work as expected. What is wrong with the circuit and how would you correct the mistake? *(5 marks)*

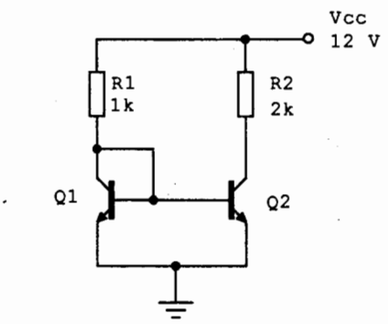

Fig.Q2a

(b) For the Widlar current source circuit shown in Fig. Q.2b, the transistors are matched and β may be assumed to be >> 1 unless otherwise stated.

(i) Show that $I_o = \frac{V_T}{R_E} \ln\left(\frac{I_{ref}}{I_o}\right)$ *(5 marks)*

(ii) Design the current source so that I_o = 400 μA using ±15 V supplies. Resistor values used should not exceed 20 kΩ. *(5 marks)*

(iii) What is the maximum load resistance that can be connected to your current source in (ii)? *(4 marks)*

(iv) Calculate the output resistance of your current source when the transistors used have β=100 and V_A = 100 V. *(6 marks)*

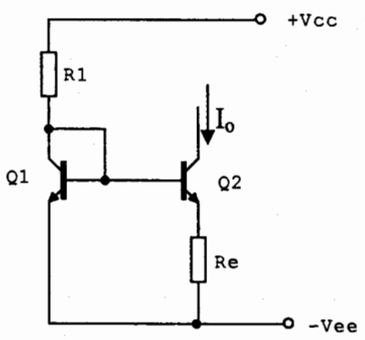

Fig.Q2b

QUESTION THREE

(a) **(i)** Derive an expression which can be used to calculate the input offset voltage due to mismatch in the collector resistors of a basic BJT differential amplifier, assuming that $\alpha = 1$ and that all transistors are matched.. *(5 marks)*

(ii) Use your expression to evaluate the mismatch in a BJT differential amplifier with a total bias current of 500 μA when collector resistors have tolerances of ±2%. *(2 marks)*

(iii) If emitter degeneration resistors with $R_E = 8r_e$ are added what input offset voltage results? *(4 marks)*

(b) Figure Q.3b shows a differential amplifier whose gain is controlled by a dc voltage V_c.

(i) Using the exponential I-V equation of a BJT in active mode and the relationships between the currents and voltages shown in the diagram, show that under steady state conditions the current I_3 is given by

$$I_3 = \frac{V_o}{R_1} - \frac{V_{BE4}}{2R_2} + \left(\frac{1}{2R_2} - \frac{1}{R_1}\right)V_c$$ *(5 marks)*

(ii) Explain how the voltage V_c controls the gain of the amplifier. *(3 marks)*

(iii) Using the relationship in (i) explain how can the output voltage can be made independent of V_c while the amplifier is stabilizing after a change in V_c? *(2 marks)*

(iv) Obtain expressions for the g_m and gain of the amplifier in terms of V_c and the circuit parameters. *(4 marks)*

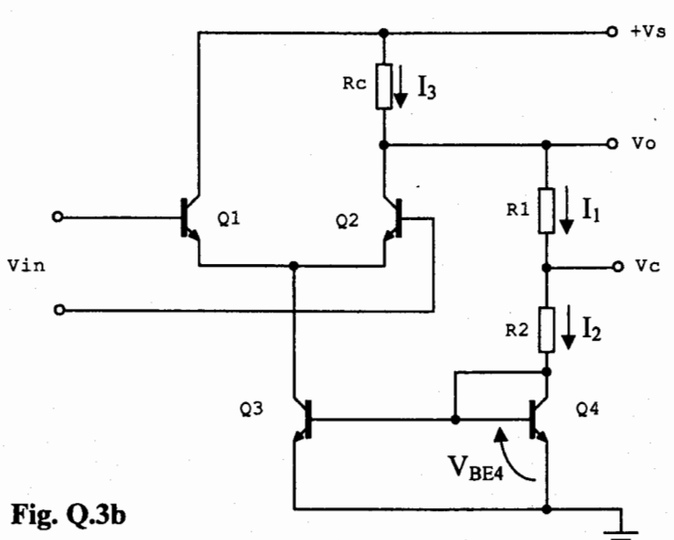

Fig. Q.3b

QUESTION FOUR

(a) A MOSFET with constant V_{GS} operating in the saturation region is found to have $i_D = 1.8$ mA at $v_{DS} = 5$ V and $i_D = 1.85$ mA at $v_{DS} = 7$ V. Using a sketch of output characteristics (i_D vs v_{DS}) of a MOSFET use this data to calculate the corresponding values of r_o, V_A and λ for this MOSFET. *(4 marks)*

(b) A MOSFET biased as shown in Fig. Q.4b has $k_n'\left(\frac{W}{L}\right) = 1$ mA/V^2.

(i) What value of R_S should be used to get $v_D = 2$ V. Specify R_S to 1 significant digit. *(6 marks)*

(ii) Find the actual value of v_D when the resistor accurate to 1 significant digit found in (i) is used. *(6 marks)*

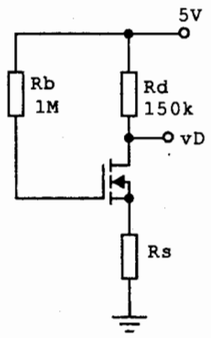

Fig Q.4b

(c) Determine the output current at $V_o = 5$ V for the MOS current mirror given in Fig. Q.4c. The transistors used have $V_{t1} = V_{t2} = 1$ V, $\lambda_1 = \lambda_2 = 0.02$ V^{-1}, and $k_n'\left(\frac{W}{L_1}\right) = 200$ μA/V^2, $k_n'\left(\frac{W}{L_2}\right) = 300$ μA/V^2. *(9 marks)*

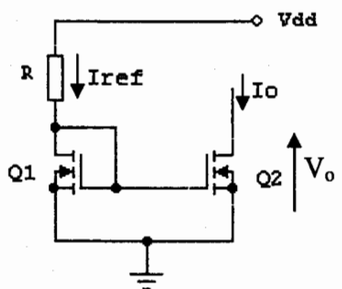

Fig Q.4c

QUESTION FIVE

(a) Figure Q.5a shows a simplified input stage of the NE592 video amplifier. This input stage is followed by another differential stage and emitter followers so that the overall gain of the IC with terminals G1A and G1B connected is $g_m k R_L' = 400$ where g_m is transconductance of the input stage, R_L' is the effective differential load impedance on the input stage and k is the gain of the subsequent stages after the input stage. Through use of the gain select terminals G1A, G1B, G2A and G2B the gain can be varied between 0 (minimum) and 400 (maximum) by shorting, open-circuting or connecting external R or RLC circuits to terminals G1A and G1B, or G2A and G2B. In summary, the gain depends on the g_m of the input stage.

(i) What is the gain when all gain select terminals are left open? *(2 marks)*

(ii) What is the gain of the amplifier when terminals G1A and G1B are shorted. *(2 marks)*

(iii) Estimate the gain of the amplifier when terminals G2A and G2B are shorted *(6 marks)*

(iv) Estimate the gain of the amplifier when a resistor of 1 kΩ is connected between G2A and G2B. *(2 marks)*

(v) The series RLC circuit shown in Fig. Q.5a is connected between G1A and G1B. Find an expression for the g_m of the input stage and the variation of the gain of the amplifier with frequency. Sketch the gain-frequency characteristic. *(6 marks)*

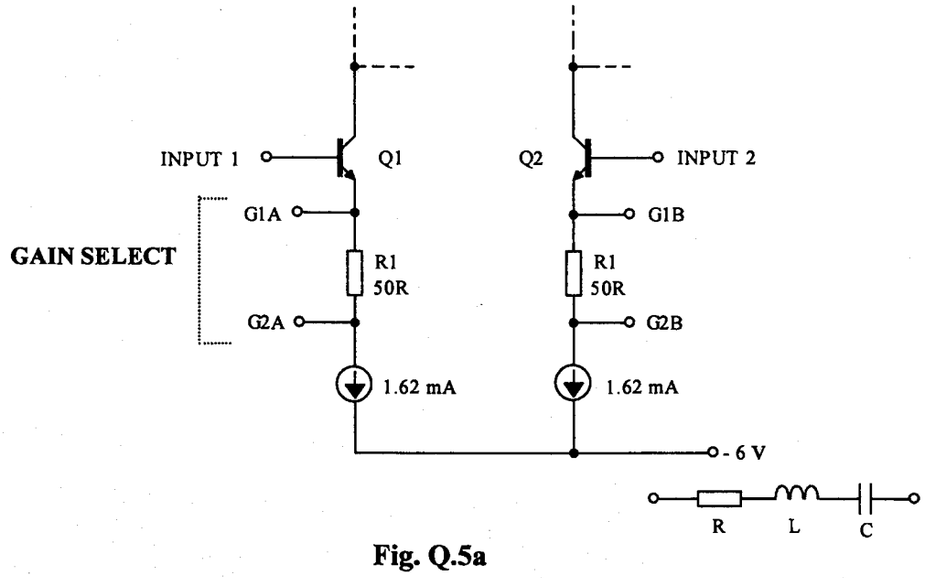

Fig. Q.5a

Question 5 continued

(b) (i) Sketch a CMOS logic gate realization of the function

$$Y = A + B(C + D)$$ *(5 marks)*

(ii) How many transistors does it need? *(2 marks)*

END OF EXAMINATION PAPER

SOME USEFUL MOSFET EQUATIONS

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \text{ in triode region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \text{ in saturation region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 (1 + \lambda v_{DS}) \text{ in saturation region with Channel Modulation effect}$$

BJT EBERS-MOLL EQUATIONS

$$i_E = \frac{I_s}{\alpha_F}\left(e^{v_{BE}/V_T} - 1\right) - I_s\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_C = I_s\left(e^{v_{BE}/V_T} - 1\right) - \frac{I_s}{\alpha_R}\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_B = \frac{I_s}{\beta_F}\left(e^{v_{BE}/V_T} - 1\right) + \frac{I_s}{\beta_R}\left(e^{v_{BC}/V_T} - 1\right)$$