UNIVERSITY OF SWAZILAND

SUPPLEMENTARY EXAMINATIONS JULY 2007

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRONIC ENGINEERING

TITLE OF PAPER: ANALOGUE ELECTRONICS III

COURSE NUMBER: E511

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. **Answer any <u>FOUR</u> (4) of the following five questions.**
2. **Each question carries 25 marks.**
3. **Unless otherwise stated, $V_{BE(ON)} = 0.7$ V and $V_T = 0.025$ V.**
4. **If you think not enough data has been given in any question you may assume reasonable values.**
5. **A sheet containing some useful equations is attached at the end of the examination paper.**

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS EIGHT (8) PAGES INCLUDING THIS PAGE

QUESTION ONE

(a) In the circuit shown in Fig Q.1a, the transistors may be assumed to be matched with each with a current gain β.

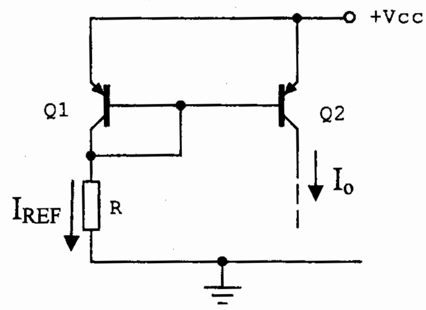
(i) Obtain an accurate expression for the relationship between the currents I_{REF} and I_o. *(3 marks)*

(ii) If β=120, evaluate the error in assuming that $I_{REF} = I_o$. *(2 marks)*

(iii) Name two possible applications of this circuit as a circuit building block. *(2 marks)*

(iv) What are the drawbacks when using this circuit in the applications you mentioned in (iii)? *(4 marks)*

Fig. Q.1a



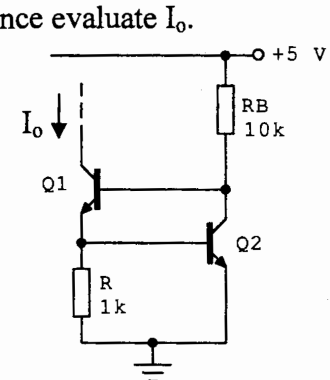
(b) Consider the circuit shown in Fig. Q.1b.

(i) What is the voltage at the base of transistor Q1? *(2 marks)*

(ii) Evaluate the current in resistor R_B. *(1 mark)*

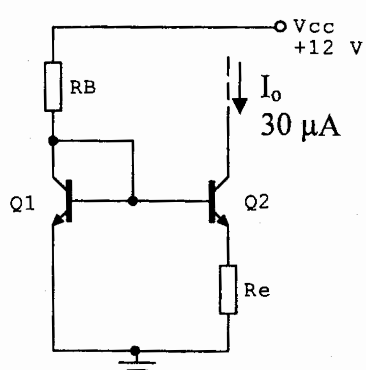
(iii) If the effects of finite β values are ignored, and the transistors are assumed to be operating in the active region, show that the current I_o is independent of the supply voltage and hence evaluate I_o. *(4 marks)*

Fig. Q 1b



(c) For the the Widlar current source shown in Fig. Q1c. determine the required values of resistors so that the circuit gives a constant output current I_o of 30 μA. The transistors are matched and specified to have V_{BE} = 0.7 V at 1 mA. *(7 marks)*

Fig. Q.1c



QUESTION TWO

(a) A diode has $V_D = 0.7$ V at 1 mA and is characterized by n = 1. It is connected in series with a 100-Ω resistor to a 3.3 V dc supply. Using iterative analysis and the exponential diode model, give an accurate estimate (to 4 significant figures) of the current through the diode. *(12 marks)*

(b) For the circuit in Fig. Q.2b,

(i) Explain why the current in R1 is equal to the forward current in the diode. *(3 marks)*

(ii) Hence or otherwise, obtain an expression for V_o in terms of V_{in} and the diode parameters. *(5 marks)*

(iii) Over what range of values of V_{in} will the circuit perform as expected? *(1 mark)*

(iv) The diode is replaced with an NPN BJT with a grounded base and the collector connected to where the anode of the diode was and the emitter to the output. Show that the relationship between the V_o and V_{in} is of the same form as found in b(ii). *(4 marks)*

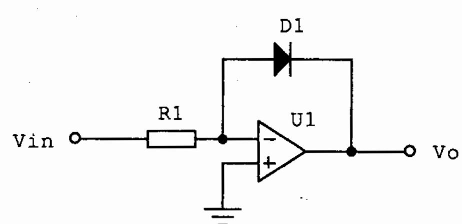


Fig. Q.2b

QUESTION THREE

(a) For the BJT in Fig.Q.3a assume that β=150.

(i) Find the value the bias resistor R_b for the BJT to be on the edge of saturation (EOS). Assume $V_{CE(EOS)} = 0.3$ V *(6 marks)*

What would happen to the operation mode of the transistor in each of the following alterations:

(ii) The power supply voltage is reduced. *(2 marks)*

(iii) the BJT is replaced with one of β=200. *(2 marks)*

(iv) R_b is increased from the value you evaluated in a(i). *(2 marks)*

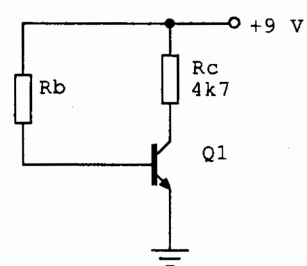


Fig. Q. 3a

(b) **(i)** "The Early Effect limits the output resistance of a BJT". Explain this statement. *(7 marks)*

(ii) Calculate the collector current and ouput resistance of a BJT with $V_A = 80$ V, $I_b = 13.5\ \mu A$, $\beta = 180$ and $V_{CE} = 6$ V. *(6 marks)*

QUESTION FOUR

(a) The n-channel enhancement mode MOSFET current mirror in Fig. Q4a are identical with $V_t = 1$ V and $\frac{1}{2}\frac{W}{L}\mu C_{ox} = 0.2$ mA/V^2.

(i) Determine V_{GS}. *(6 marks)*

(ii) Determine I_o. *(2 marks)*

(iii) Determine the allowable range of V_o for the mirror to function properly. *(2 marks)*

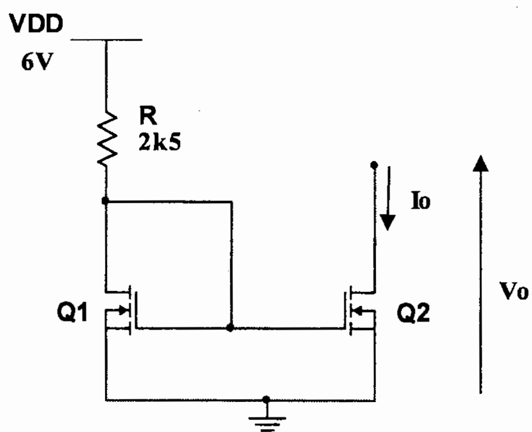


Fig Q 4a

(b) For the circuit shown in Fig. Q 4b, estimate the value of the voltage V_o. You may neglect the effect of finite base currents. *(4 marks)*

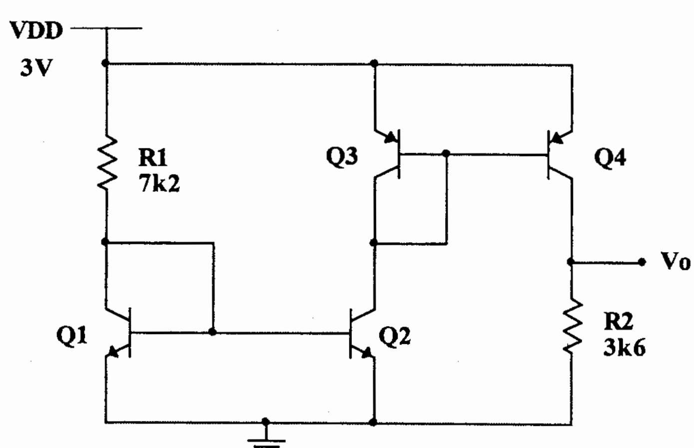


Fig. Q4b

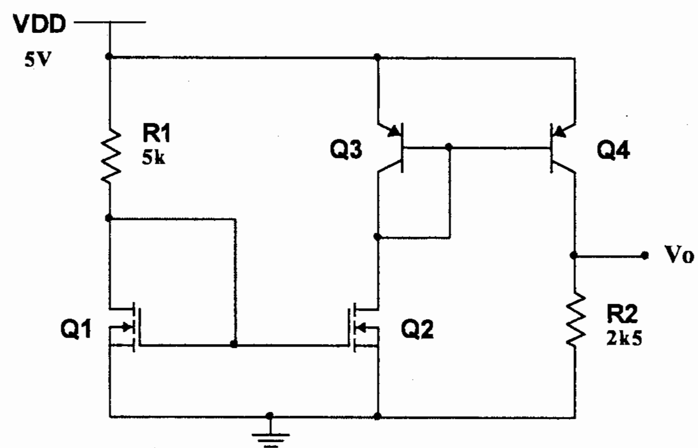
Question Four (Continued)

(c) For the circuit shown in Fig. Q.4c the BJTs have a finite β = 100 and the MOSFETS have $V_t = 1$ V and $\frac{1}{2}\frac{W}{L}\mu C_{ox} = 0.1$ mA/V^2.

(i) Assuming that Q1 and Q2 are in saturation mode, estimate the value of the current through R1. *(2 marks)*

(ii) Show that Q1 and Q2 actually operate in the saturation mode. *(5 marks)*

(iii) Find the value of the output voltage Vo. *(4 marks)*



QUESTION FIVE

(a) (i) Sketch a CMOS logic gate realization of the function

$$Y = B(\overline{A} + D) + \overline{C}$$ *(7 marks)*

(ii) How many transistors does it need? *(2 marks)*

(b) A differential amplifier circuit with a differential input and a single-ended output is shown in Fig. Q5b. The transistors used are matched with $V_A = 100$ V and $\beta=100$.

(i) Estimate the gain $\frac{v_o}{v_1 - v_2}$. *(8 marks)*

(ii) Find the differential input resistance. *(3 marks)*

(iii) What values of emitter degeneration resitors, R_E, are required to double the differential input resistance? *(2 marks)*

(iv) Find the new gain after (b)(iii) is implemented. *(3 marks)*

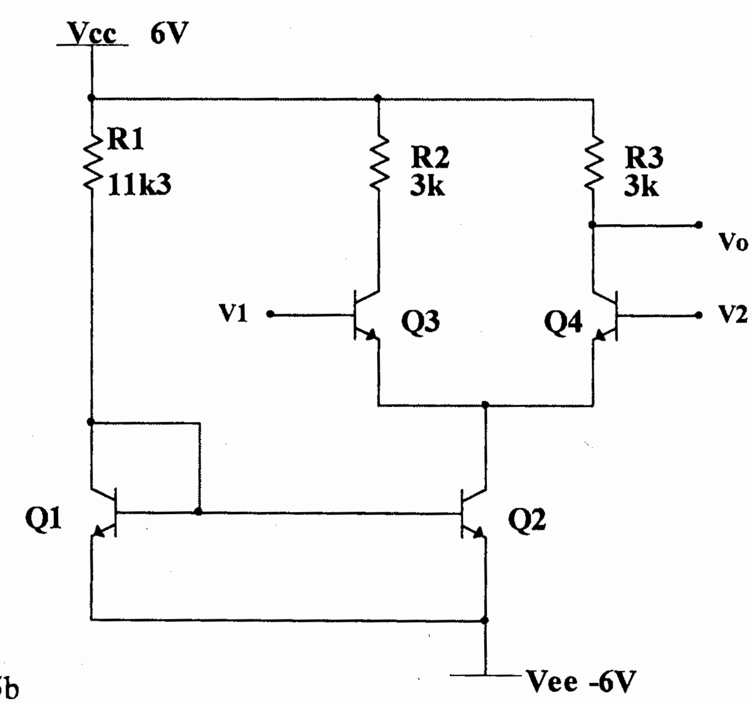


Fig. Q.5b

=== END OF EXAMINATION PAPER, SOME USEFUL EQUATIONS FOLLOW ===

SOME USEFUL MOSFET EQUATIONS

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \text{ in triode region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \text{ in saturation region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 (1 + \lambda v_{DS}) \text{ in saturation region with Channel Modulation effect}$$

BJT EBERS-MOLL EQUATIONS

$$i_E = \frac{I_s}{\alpha_F}\left(e^{v_{BE}/V_T} - 1\right) - I_s\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_C = I_s\left(e^{v_{BE}/V_T} - 1\right) - \frac{I_s}{\alpha_R}\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_B = \frac{I_s}{\beta_F}\left(e^{v_{BE}/V_T} - 1\right) + \frac{I_s}{\beta_R}\left(e^{v_{BC}/V_T} - 1\right)$$