UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRONIC ENGINEERING

MAIN EXAMINATION MAY 2008

TITLE OF PAPER: **INTRODUCTION TO ANALOG & DIGITAL ELECTRONICS**

COURSE CODE: **E212**

TIME ALLOWED: **THREE** HOURS

INSTRUCTIONS:

1. Answer question **one** and any other **three** questions.
2. Question one carries 40 marks.
3. Questions 2, 3, 4, and 5 carry 20 marks each.
4. Marks for different sections are shown in the right-hand margin

This paper has 6 pages including this page.

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Question 1

A) A reference voltage of 3 V is required to drive a circuit which has an effective input resistance of $R_2 = 200\Omega$. The reference voltage is to be produced from a supply voltage V which can vary between 4 and 4.5 V. A suitable circuit might be that shown in Figure 1A. The zener voltage V_z is 3 V. Calculate :

(I) the current I_L flowing in the load resistor R_2. [2 marks]

(II) value of the resistor R [3 marks]

(III) the maximum power dissipated in the zener or the power rating of the zener. [4 marks]

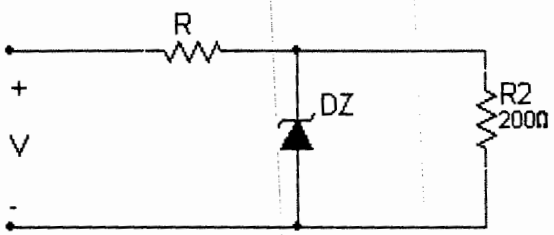


Figure 1A

B) (I) Write in binary the decimal (56.21). [5 marks]

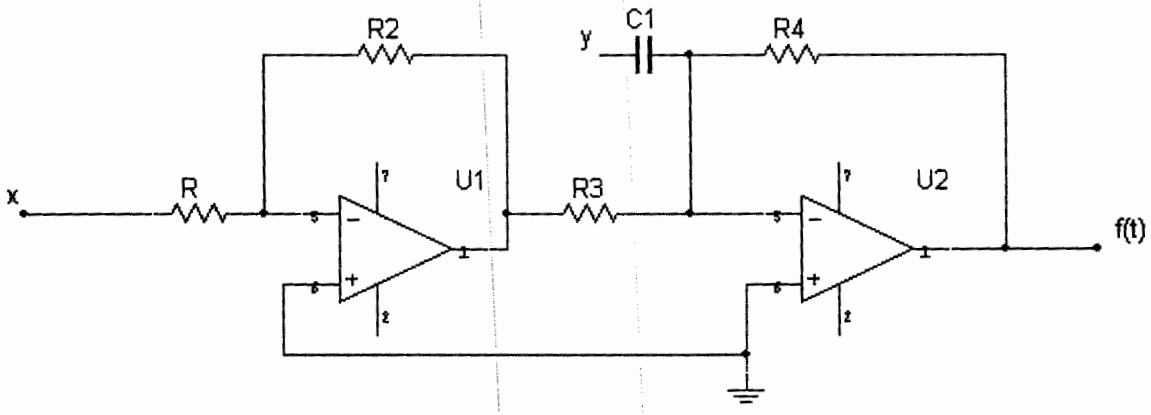
(II) Write in decimal the binary (11011.001). [3 marks]

(III) Simplify the boolean equations $X = C.(A + \overline{B}.(\overline{D} + E + \overline{C}) + \overline{B}.C) + A$;

$$Y = (ABC + C).(A + B).\overline{A}$$

[8 marks]

C) (I) Derive an expression for the output f(t) of the circuit shown in Figure 1C. [5 marks]



Note: R = R3 =R4 ; R2 = 8xR

Figure 1C

II) Design a summing amplifier to perform the following operation

$$V_{out} = V_1 + 5V_2 + 2V_3.$$ [10 marks]

Question 2

For the common emitter circuit shown in Figure 2, $\beta = 79$, $V_{BEQ} = 0.6V$, $R_1 = 139\ k\Omega$, $R_1 = 1k\Omega$, and $R_3 = 72\ \Omega$

(A) Find the voltage V_{CEQ} and current I_{CEQ}. [10 marks]

(B) Draw the equivalent small signal simplified hybrid-π circuit. [5 marks]

(C) With $g_m = 40 I_{EQ}$ and $r_\pi = \dfrac{\beta}{g_m}$ determine the voltage gain $\dfrac{v_o}{v_{in}}$ [5 marks]

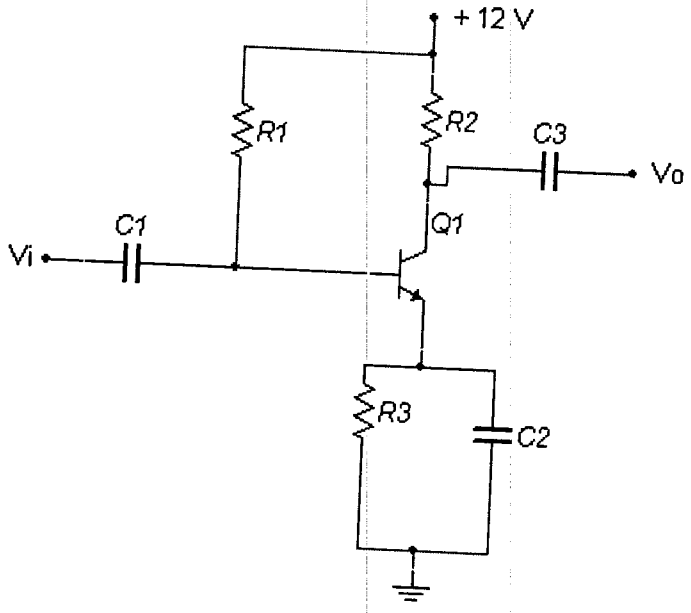


Figure 2

Question 3

A) Sketch the input characteristic of a Bipolar Junction Transistor for a common-emitter configuration. [6 marks]

B) Sketch the output characteristic of a Bipolar transistor for a common-emitter configuration. Label the Saturation and Active regions [10 marks]

C) What is the major difference in how BJT's and FET's operate? [4 marks]

Question 4

For the logic circuit shown in Figure 4,
A) Derive a Boolean expression to describe its operation and simplify your expression. [16 marks]

B) Draw a truth table of Q = A + BC. [4 marks]

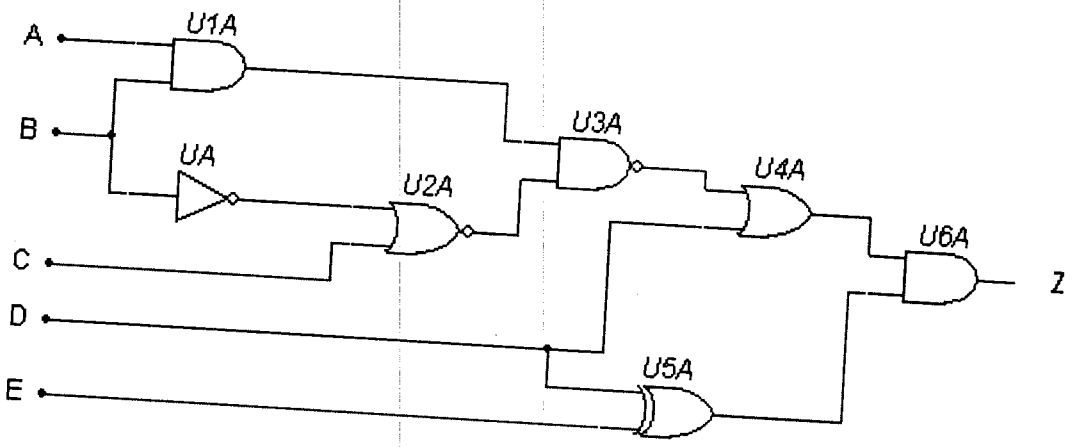


Figure 4

Question 5

A 2N5486 n-channel JFET has pinch-off voltage of - 6V and I_{DSS} = 14 mA. When this transistor is used in the circuit shown in Figure 5, the drain voltage is 7 V and R_D = 2 kΩ. Calculate

A) the value of I_D [3 marks]

B) the value of V_{GS} [4 marks]

C) the value of the resistor R_s. [3 marks]

D) If g_m = 0.002 and r_d = 100kΩ then draw the small signal equivalent circuit and obtain the voltage gain v_o/v_i. [10 marks]

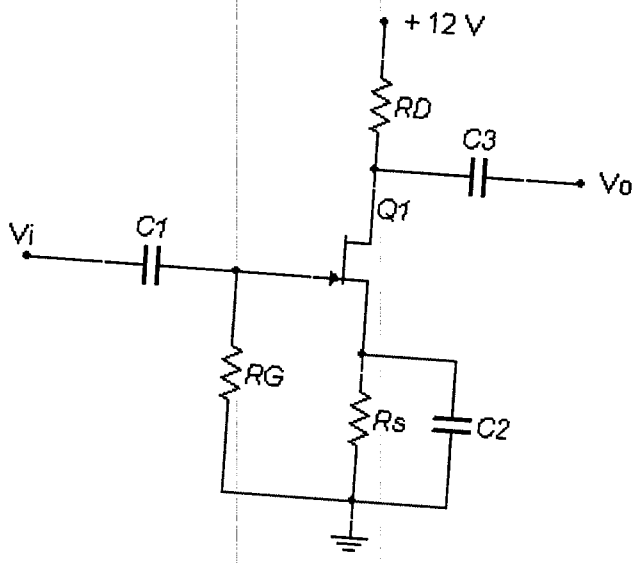


Figure 5