UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

MAIN EXAMINATION
December 2007

Title of the Paper: **ELECTRONICS II**
Course Number: **E441**
Time Allowed: **Three Hours**.

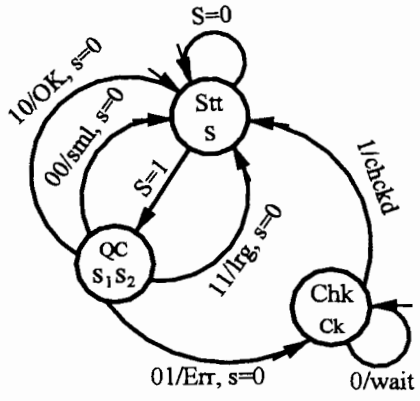
Instructions:
1. To answer, pick any five out of seven questions in the following pages.
2. Each question carriers 20 points.
3. This paper has 8 pages, including this page.

DO NOT OPEN THE PAPER
UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

ASM Chart:

Q1a 10pts: Convert the given state diagram on the right into an ASM chart.

Q1b 10pts: Drive an ASM table from the given state diagram on the right.



Registers and Counters:

Q2a 10pts: Draw a block diagram to show all control signals, data inputs, and data outputs of a universal binary register. If use codes to select the control functions, you can by yourself define the function codes.

Q2b 10pts: For a universal binary register, describe, using block diagram circuit, how you do serial input of a 4-bit data. All control signals must be properly set and shown on the circuit diagram. Because of inputting only 4 bits, you must have a circuit to control the number of clocks. This circuit is called word time control.

Register-Transfer Circuit:

Q3 It is required to exchange two data of 16_{dec} bytes in the computer memory M(10-1F) and M(30-3F). Use accumulator regA as the intermediate storage device. The regA and RAM are of the same byte size (for example, 4 bits) and in a common bus structure. RAM data line is bi-directional, you must have a direction control AND switch.

(a) 10pts: Draw the hardware circuit for this system. Of course, MAR, MBR, and memory unit must be included. The control unit is not necessarily in detailed circuit but a block with inputs and outputs.

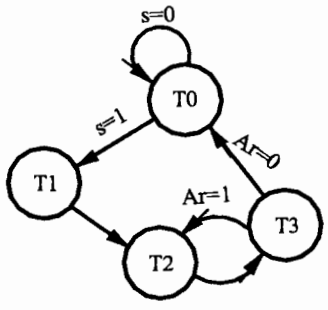
(b) 10pts: Use registry language to describe the transfer operation.

Practical design with ASM

Q4 20pts: Design an ASM chart describing the operation process of a two level elevator. The elevator has 2 buttons inside the cage to command the elevator to close the door and go up or down. (may reduce to one, but the machine must have a mechanism that command the cage automatically go to its right direction; that is, on the 1st floor to the 2nd floor, likewise on the 2nd floor to the 1st floor.) And it has one button each on the gate of each floor to call the elevator and open the door. All other operations are according to the normal commercial elevator.

Control Circuit Design

Q5 20pts: Shown on the right is a 4-state state diagram of a control unit where control inputs are s, Ar and no external outputs but from the state itself to command registry transfer operations. Here in this control circuit, registry transfer operations are not concerned. Design the control circuit by the PLA structure with two D ffs G_2 and G_1 as the state memory.



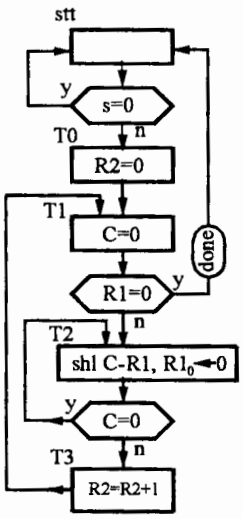
Q6 20pts: Shown on the right is a flow chart of a digital system that counts the 1's in the register R1 and the total count is stored in R2. Appended on the left to R1 is a one bit carry register C, shown in T2 state in the figure. "s" is a start switch.

(a). List the register transfer statements executed in each control state,

(b). Draw a state diagram for the control,

(c). Design the control circuit by the one ff per state structure,

(d). Draw the whole circuit of the system in the block diagram form.



Micro-Operation and Simple Computer:
Q7 An instruction is specified as follows:

Mnemonic	Description	Function
ADD R	Add R to RegA	A←A+R

(a) 10pts: List the sequence of micro-operations (given in the textbook) for executing this instruction. Note the operation is that a constant in the register R is added into the accumulator A in the CPU.

(b) 10pts: Design, with blocks, the circuit required to perform this instruction. This circuit is not meant to be a general computer but a circuit sufficient for this instruction only. All control signals must be included and marked.