UNIVERSITY OF SWAZILAND

SUPPLEMENTARY EXAMINATIONS 2007/8

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE ELECTRONICS III
COURSE NUMBER:	E511
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. **Answer any <u>FOUR</u> (4) of the following five questions.**
2. **Each question carries 25 marks.**
4. **If you think not enough data has been given in any question you may assume reasonable values.**
5. **A sheet containing some useful equations and other data is attached at the end of the examination paper.**

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE (*25 marks)*

(a) In what mode should the BJTs of a basic current mirror operate? *(1 mark)*

(b) A designer produced the circuit shown in Fig. Q.1b. Assume that the transistors are matched. On testing the circuit it is found that is not operating properly. What is wrong with the circuit? How would you correct the mistake(s)? *(6 marks)*

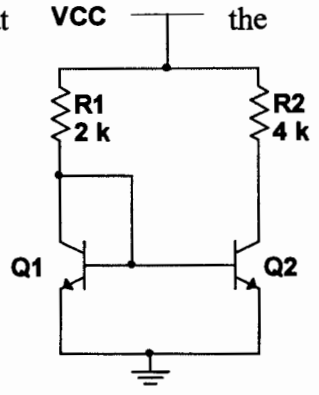

Fig. Q1b

(c) For the circuit shown in Fig. Q.1c assume that the transistors are matched, but the effect of the current gain β is not negligible.

(i) Find an exact expression for I_o/I_{ref} with and without the Early Effect. *(9 marks)*

(ii) Given that $I_{ref} = 1$ mA, $V_{BE} = 0.7$ V, $V_{A2} = 75$ V, $\beta = 100$ and $V_o = 10$ V, find I_o. *(2 marks)*

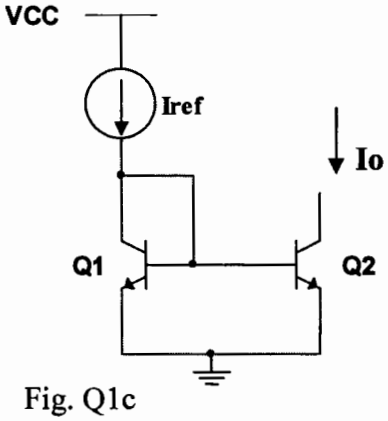

Fig. Q1c

(d) Explain why the circuit in Fig. Q.1d is better than that of the basic current mirror. *(7 marks)*

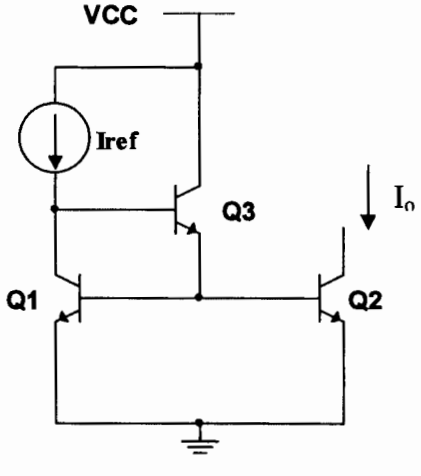

Fig. Q1d

QUESTION TWO ***(25 marks)***

(a) An NMOS transistor circuit is shown in Fig. Q.2a. The transistor has

$V_t = 0.8$ V, $\mu_n C_{ox} = 200\ \mu$A/V^2, $\frac{W_1}{L_1} = 25$ and λ=0

Find R_D and R_S so that the NMOS operates at I_D = 0.5 mA and V_D = 1.0 V with respect to ground. *(12 marks)*

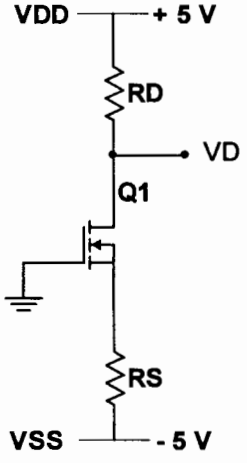

Fig. Q2a

(b) The NMOS transistor in Fig Q.2b is to be designed to operate with V_D = 0.2 V with respect to ground . The transistor parameters are:

$V_t = 1$ V, $k_n' \frac{W_1}{L_1} = 2$ mA/V^2 and λ=0

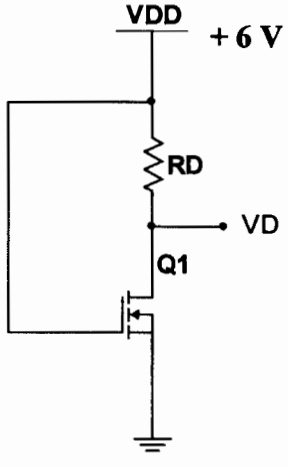

Fig. Q2b

(i) In what mode should the transistor be operating with the desired V_D? *(2 marks)*

(ii) Specify the value of R_D to meet the design condition. *(7 marks)*

(iii) What is the effective r_{DS} of the transistor with this operating condition?

(4 marks)

QUESTION THREE ***(25 marks)***

(a) Neglecting base currents show that the output d.c voltage V_o of the circuit in Q. 3a is approximately 0 V. *(10 marks)*

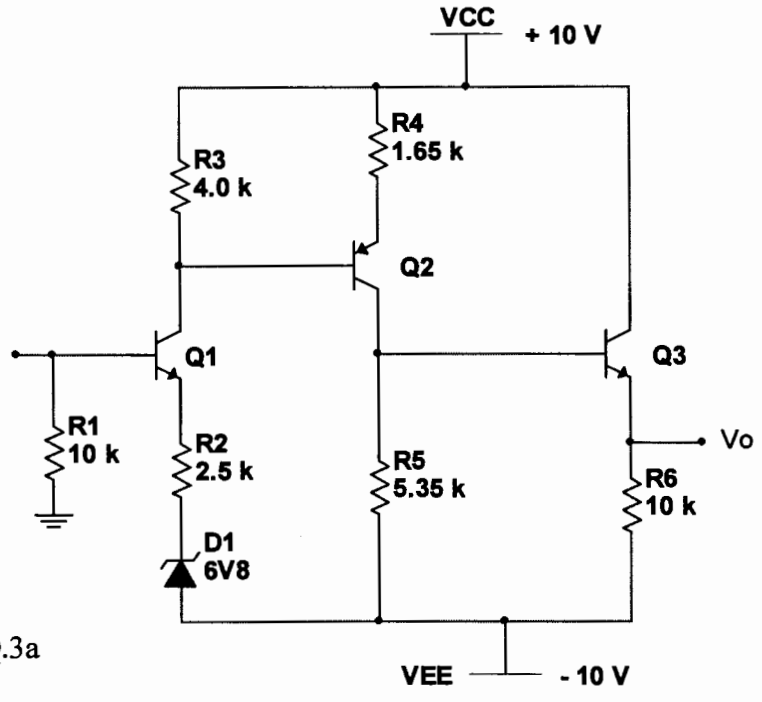

Fig. Q.3a

(b) A diode and a resistor of 300 Ω are connected in series to a 1.6 V d.c. power supply. The diode is specified as having $V_D = 0.7$ V at $I_D = 1$ mA.

(i) Find a rough estimate of the current in the diode. *(2 marks)*

(ii) If the diode has $n = 2$, find a more accurate value (with 3 significant figure accuracy) for the current and voltage across the diode using an iterative procedure. Note that you must work with 4 significant figures to get a result accurate to 3 significant figures.

(13 marks)

QUESTION FOUR ***(25 marks)***

(a) A BJT differential amplifier has 300 μA bias (tail) current.

(i) Find the g_m of each BJT and the differential input resistance. *(4 marks)*

(ii) Explain two methods by which the input resistance may be increased by a factor of 4. What are the consequences of using each of the methods you have given? *(6 marks)*

(b) For the BJT differential amplifier shown in Fig. Q.4b calculate

(i) The differential input resistance, assuming β = 100. *(3 marks)*

(ii) The differential voltage gain. *(2 marks)*

(iii) The common mode gain assuming perfect matching. *(2 marks)*

(iv) The CMRR. *(2 marks)*

(v) The minimum common mode gain due to use of ±1.5% tolerance resistors at the collectors. Neglect the effect of R_{ee}. *(6 marks)*

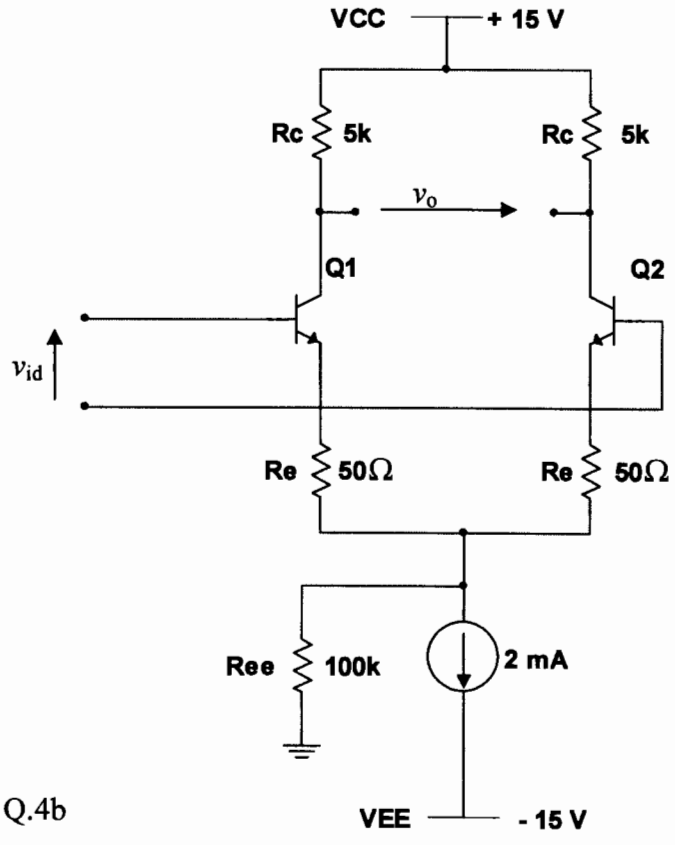

Fig. Q.4b

QUESTION FIVE ***(25 marks)***

(a) Assuming that the base currents are negligible, calculate the collector currents and collector voltages of all the transistors in the circuit shown in Fig. Q.5a. *(12 marks)*

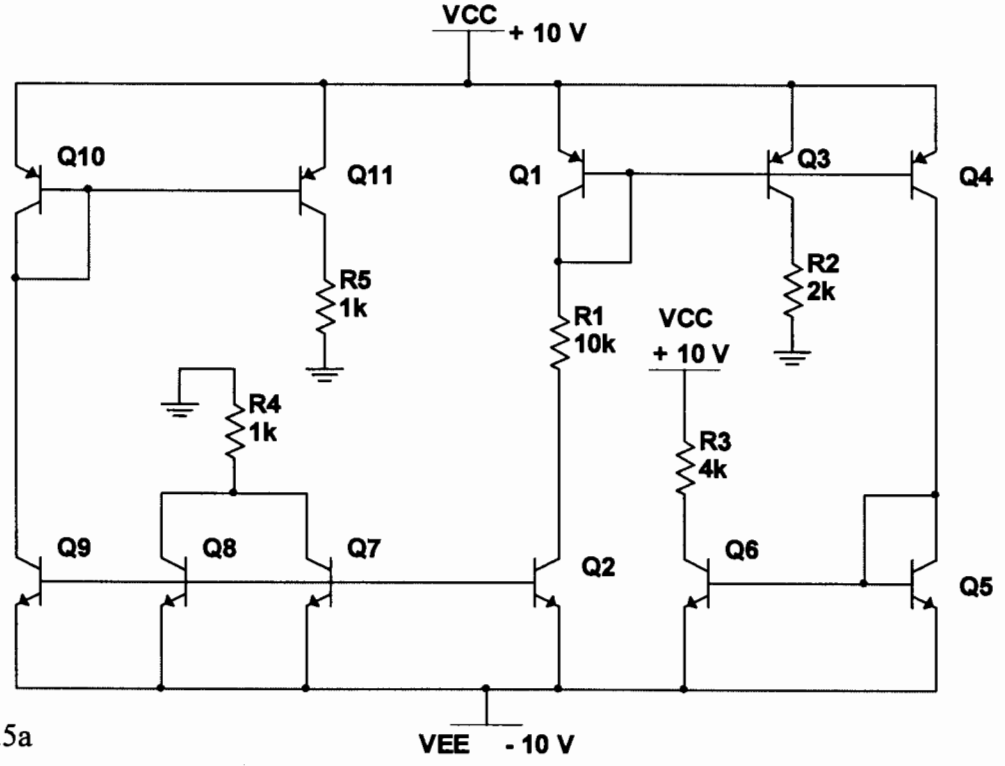

Fig. Q.5a

(b) (i) What is the functional difference between enhancement type and depletion type NMOS transistors? *(4 marks)*

(ii) Obtain the truth tables for the logic function F of the digital NMOS circuits shown in Fig. Q.5b. *(9 marks)*

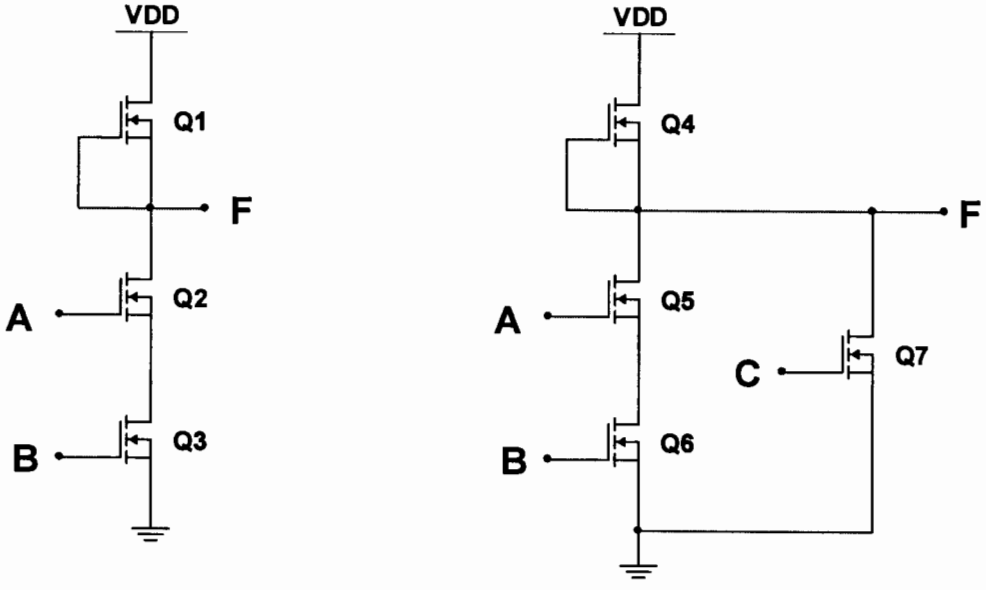

Fig Q.5b

1. SOME USEFUL MOSFET EQUATIONS

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \text{ in triode region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \text{ in saturation region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 (1 + \lambda v_{DS}) \text{ in saturation region with Channel Modulation effect}$$

2. BJT EBERS-MOLL EQUATIONS

$$i_E = \frac{I_s}{\alpha_F}\left(e^{v_{BE}/V_T} - 1\right) - I_s\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_C = I_s\left(e^{v_{BE}/V_T} - 1\right) - \frac{I_s}{\alpha_R}\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_B = \frac{I_s}{\beta_F}\left(e^{v_{BE}/V_T} - 1\right) + \frac{I_s}{\beta_R}\left(e^{v_{BC}/V_T} - 1\right)$$

3. Unless otherwise stated, $V_{BE(ON)} = 0.7$ V and $V_T = 0.025$ V.