UNIVERSITY OF SWAZILAND
FACULTY OF SCIENCE
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

MAIN EXAMINATION 2009

TITTLE OF PAPER: **INTRODUCTION TO ANALOG & DIGITAL ELECTRONICS**

COURSE CODE: **E212**

TIME ALLOWED: **THREE** HOURS

INSTRUCTIONS:

1. Answer **any four** of the following **five** questions.
2. Each question carries 25 marks
3. Marks for different sections are shown in the right hand margin

This paper has 6 pages including this page

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Question 1

A) Explain, with reference to a semiconductor material the difference between *diffusion* current and *drift* current. **(4 marks)**

B) With the aid of suitable diagrams, describe the structure of a p-n junction diode as well as reverse and forward biasing of the diode. **(10 marks)**

C) A semiconductor diode, the forward and reverse characteristics which can be considered ideal, is used in a half-wave rectifier circuit supplying a resistive load of 1000 Ω.

i) if the r.m.s value of the sinusoidal voltage is 250V, determine the peak diode current and the r.m.s diode current. **(3 marks)**

ii) Describe with the aid of suitable diagrams, the rectifier action of a semiconductor. **(8 marks)**

Question 2

A For the circuit shown in **figure 2**, the input voltage $v_s = 2\sin(100\pi t)$, the potential barrier of the diode $V_d = 0.5$ volts, and $R = 100\Omega$.

i) What is the period of the input voltage? **(2 marks)**

ii) Find the voltage drop across R. **(3 marks)**

iii) Find the current through R. **(3 marks)**

iv) Compute the average value of the current through R. **(4 marks)**

v) Sketch the current waveform through the resistor R. **(3 marks)**

vi) State the effect of connecting a capacitor in parallel with the resistor R. Sketch the waveform of the voltage across the resistor R in this case. **(3 marks)**

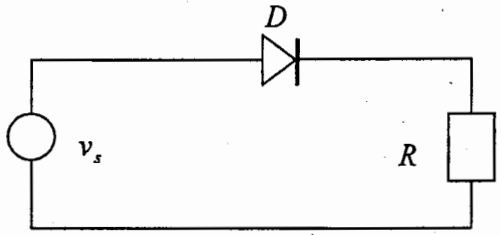


Figure 2

B i) Explain with the appropriate formulas the difference between **average value** and **root mean square** value of an alternating current. **(4 marks)**

ii) Find the average value of the wave form in **figure 3**. **(3 marks)**

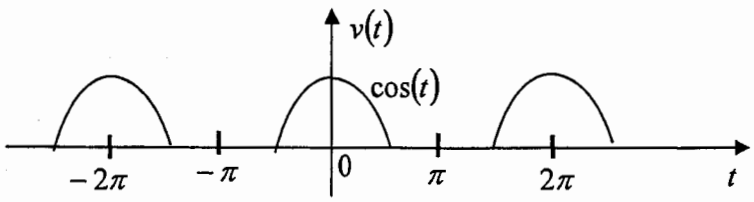


Figure 3

Question 3

A i) Differentiate between minority and majority carriers in a semiconductor device. **(6 marks)**

ii) What do you understand by the term *transfer characteristic* as applied to a transistor? **(3 marks)**

iii) The transfer characteristics of a transistor connected in the common emitter mode is described by the line passing through the points $I_B = 25\mu A, I_C = 2mA$ and $I_B = 50\mu A, I_C = 4mA$. Calculate current gain factor for a *common-base* connection using this transistor? **(4 marks)**

iv) Sketch the approximate shape of the output characteristics of a common-emitter transistor for several values of steady base current. What information is derived from the slope of these curves? **(5 marks)**

B The experimental input characteristic $i_B = f(v_{BE})$ of a transistor connected in the common emitter circuit is specified by the plot of **figure 4**. Find the coefficients a_0, a_1, and a_2 defining the power approximation of the form

$$i_B = a_0 + a_1(v_{BE} - V_0) + a_2(v_{BE} - V_0)^2$$

in the vicinity of the operating point $V_0 = 0.7V$. **(7 marks)**

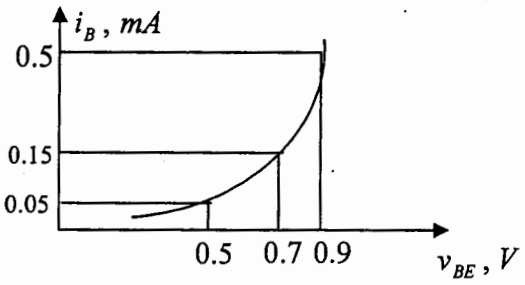


Figure 4

Question 4

A i) Describe the basic operational amplifier and give any four characteristics of an ideal operation amplifier. **(6 marks)**

ii) Explain input offset voltage when used in association with Op-Amps. **(2 marks)**

iii) With the aid of suitable diagrams describe the inverting and non-inverting operational amplifiers. For each of them derive an expression for the close loop gain. **(8 marks)**

B In the circuit diagram given in **figure 5**,

$$R_3 = 3R_1\,,\ R_4 = 5R_2\,,\ \text{and}\ R_8 = R_5 = R_6 = R_7\ .$$

Derive and expression for the output voltage V_0. **(9 marks)**

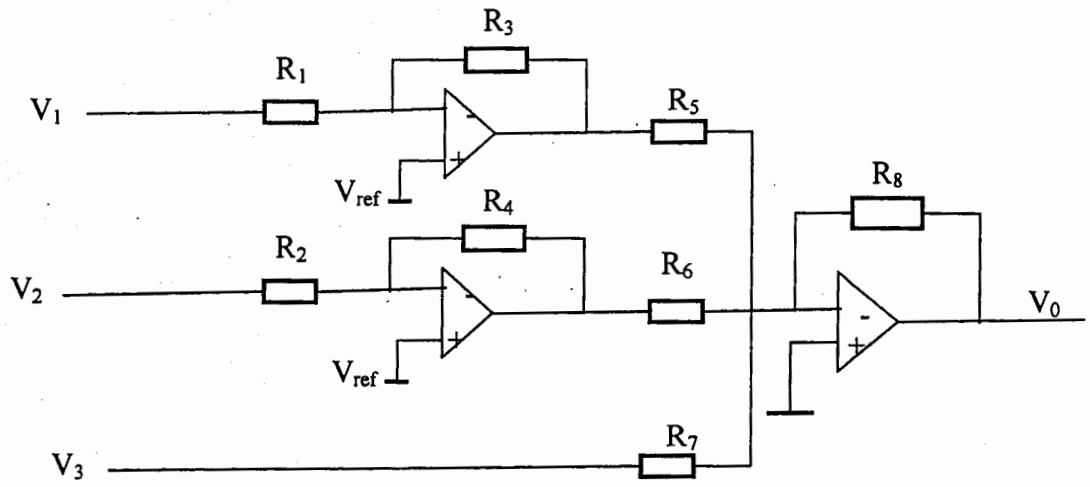


Figure 5

Question 5

A i) Subtract the decimal number 15 from 25 by binary means.

(2 marks)

ii) Add the decimal numbers 45 and 25 by binary means.

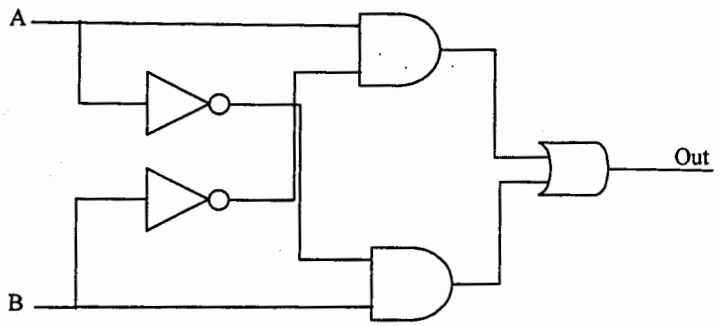
(2 marks)

B Design a logic circuit to implement the operation specified in the following Truth table **(5 marks)**

A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	1	0	1
1	1	1	0

C i) Work out the truth table of the following logic circuit.

(5 marks)



ii) Draw circuits which will generate the function

$$F = B \cdot \left(\overline{A} + \overline{C}\right) + \overline{A} \cdot \overline{B}$$

using

NOR gates **(5 marks)**

NAND gates **(5 marks)**