UNIVERSITY OF SWAZILAND
FACULTY OF SCIENCE
DECEMBER EXAMINATION 2008

TITLE OF PAPER : ANALOGUE ELECTRONICS

COURSE NUMBER : E361

TIME ALLOWED : THREE HOURS

INSTRUCTIONS : READ EACH QUESTION CAREFULLY
ANSWER ANY **FOUR** OUT OF **FIVE** QUESTIONS.
EACH QUESTION CARRIES **25 MARKS.**
MARKS FOR EACH SECTION ARE SHOWN
ON THE RIGHT-HAND MARGIN.

THIS PAPER HAS 6 PAGES INCLUDING THIS PAGE.

THIS PAPER IS NOT TO BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

QUESTION 1

(a) Figure 1 shows a common - source Field Effect Transistor amplifier with source bias impedance.

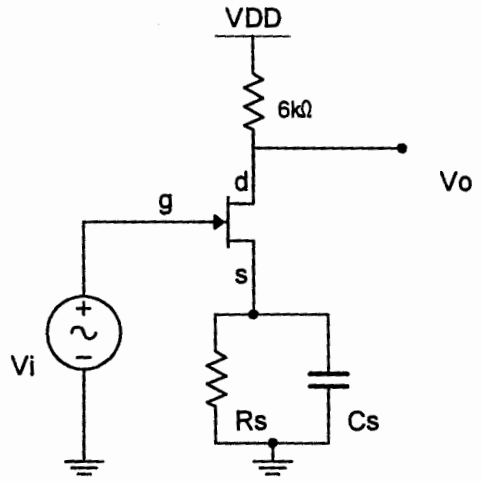

Figure 1

(i) Present the equivalent circuit of Figure 1 using the low frequency FET model.
(2 marks)

(ii) Derive an expression for the voltage gain of the circuit of (i).
(6 marks)

(b) Consider an npn transistor connected in the common - emitter configuration, with the load resistor R_L = 0.5 kΩ and the dc supply voltage V_{CC} = 10 V. The base current I_B = 40 μA and α_F = 0.995.

Compute

(i) the voltage V_{CE} when I_C = 0, and the current I_C when V_{CE} = 0.
(5 marks)

(ii) the collector current and the collector - emit V_{CC} ter voltage at the Q - point. (6 marks)

(iii) What value of resistance should be connected between the base (B) and the supply voltage (V_{CC}) to give a base current of 30 μA ?
(3 marks)

(iv) What effect will the resistance in (iii) have on the values of I_C and V_{CE} ? Show your working. (3 marks)

QUESTION 2

(a) One of the most widely used discrete - component biasing arrangement is as shown in Figure 2. Explain the function of each resistor and capacitor in the circuit.

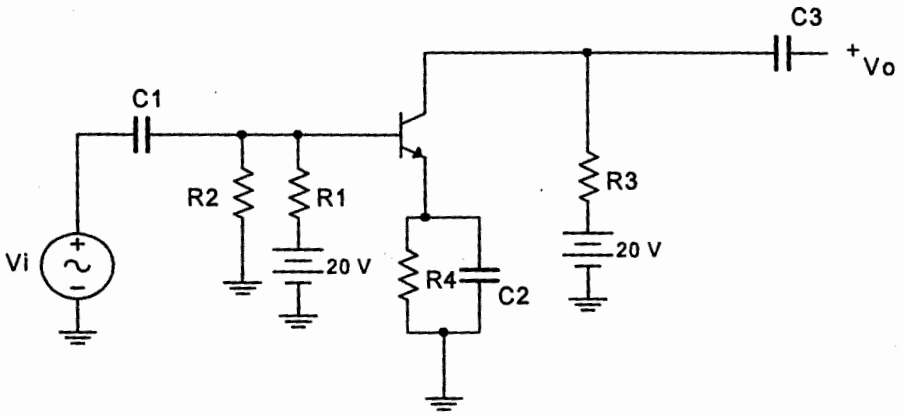

Figure 2 (6 marks)

(b) Design a common - source(CS) junction field effect transistor circuit similar to that of Figure 2. Assume that the capacitors have virtually zero reactance and can be considered short circuits at the lowest signal.

The circuit should ensure that the current I_D, is always between 5 mA and 6 mA, with V_{GS} = -0.75 V and V_{GS} = - 1.5 V, corresponding to the minimum and maximum current values, $V_{DS} \geq 8.5$ V. The supply voltage is 28 V, V_{GG} = 3 and $R_G \geq 100\ k\Omega$. V_{GG} and R_G are the Thevenin equivalent open circuit voltage and equivalent resistance of R_1 in parallel with R_2, respectively.

(19 marks)

QUESTION 3

(a) A basic, symmetrical differential amplifier uses two junction field effect transistors. Briefly explain the following terms with reference to this type of circuit.

(i) Common mode rejection ratio(CMRR). (1 mark)
(ii) Differential mode. (1 mark)
(iii) Common mode (1 mark)
(iv) The paraphase amplifier. What is the relation between its input and output signals? (2 marks)

(b) The amplifier described in (a) has a differential gain A_{DM} of 100, a common mode rejection ratio of 1000, and initial input signal levels of V_{i1} = 5.0 mV, V_{i2} = - 5.0 mV.

(i) Calculate the output voltage. (6 marks)

The signal levels are later observed to have increased to V_{i1} = 105.0 mV and V_{i2} = 95.0 mV.

(ii) What is the output voltage in this case? (5 marks)

(c) Figure 3 shows a simple current mirror circuit using two identical bipolar junction transistors, Q_1 and Q_2.

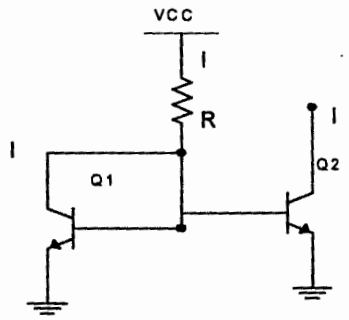

Figure 3

(d) Show the directions of the current flow and derive the expression for I_R and collector current I_C in terms of the supply voltage V_{CC} and the resistor R. (9 marks)

QUESTION 4

(a) The operational amplifier of Figure 4 has R_f = 18 kΩ and R_i = 2 kΩ.

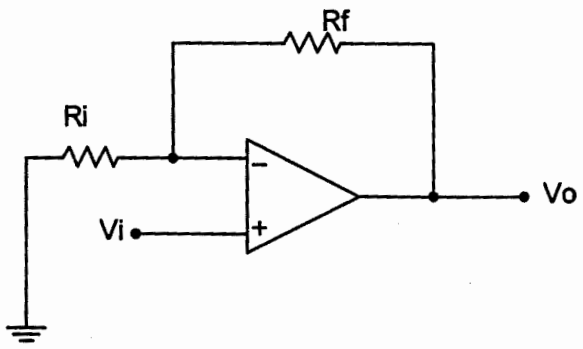

Figure 4

(a) Assuming an ideal op amp , determine

(i) the closed loop gain A_{CL} of the noninverting amplifier circuit of Figure 4.
(3 marks)

(ii) the input voltage levels at which saturation occurs, for V_{sat} = ± 13V.
(4 marks)

(b) Present circuit diagrams and derivations of expressions that relate the input voltages to the output voltages of the following circuits:

(i) an operational amplifier integrator, including any approximations used and
(8 marks)

(ii) a voltage follower circuit. Include all "error" terms and show how the expression can be simplified if the "errors" can be neglected.
(10 marks)

QUESTION 5

(a) A three - stage CE - CE - CE cascade of Figure 5.0 uses identical transistors with $\beta_F = 125$, $r_b = 0$, $V_A = \infty$ and operation is at 25°C.

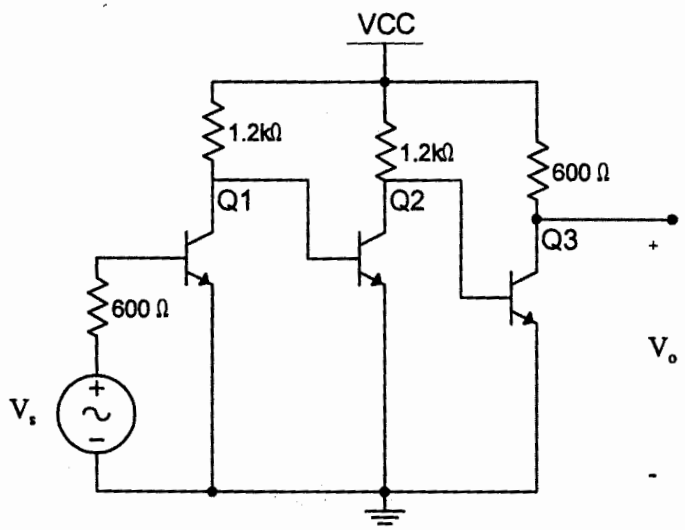

Figure 5.0

I_{CQ} = 1 mA for both Q1 and Q2, while I_{CQ} = 2 mA for Q3.
Determine the voltage gain A_v, for the amplifier of Figure 5.0.

(17 marks)

(b) Figure 5.1 shows a circuit with a silicon diode with V_γ = 0.6 V, R_f = 30 Ω. Compute the output voltage v_o and the diode voltage v_D.

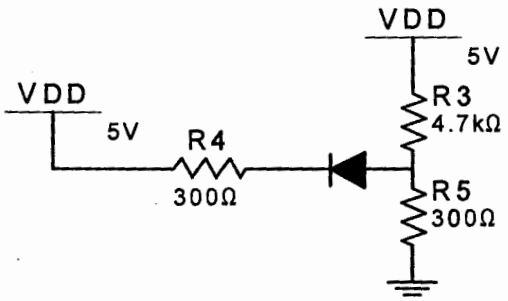

Figure 5.1 (8 marks)