UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, SECOND SEMESTER MAY 2009

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER: ANALOGUE ELECTRONICS II

COURSE CODE: E442

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. There are six questions in this paper. Answer any FIVE questions. Each question carries 20 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Show all your steps clearly in any calculations.

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THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE ***(20 marks)***

Consider the Schmitt trigger circuit shown in Fig. Q1.

(a) Defining any symbols you use, derive general equations for the triggering thresholds of the circuit. *(10 marks)*

(b) If $V_{ref} = 3$ V, $R_2 = 2R_1 = 20$ kΩ and the opamp saturates at ±12 V evaluate the thresholds and sketch the voltage transfer characteristic (v_o vs v_{in}).

(10 marks)

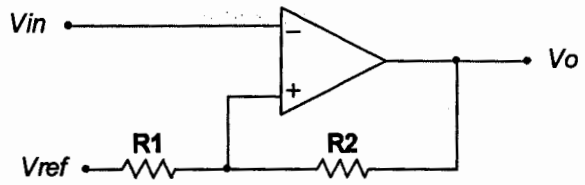


Fig. Q1

QUESTION TWO *(20 marks)*

A circuit of a Wien bridge oscillator is shown in Fig. Q2.

(a) Derive the conditions required for sustained oscillations. *(10 marks)*

(b) Given that $R_1 = 120\ k\Omega$, $R_2 = 12\ k\Omega$, $C_1 = 10\ nF$, $C_2 = 100\ nF$, find:

(i) The frequency of oscillation. *(5 marks)*

(ii) Suitable values of R_3 and R_4 for sustained oscillations to occur. *(5 marks)*

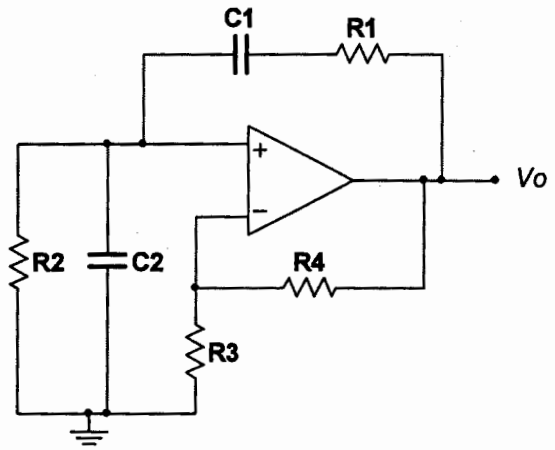


Fig. Q2

QUESTION THREE ***(20 marks)***

Figure Q3 shows a circuit of a simple FET-based Colpitts oscillator.

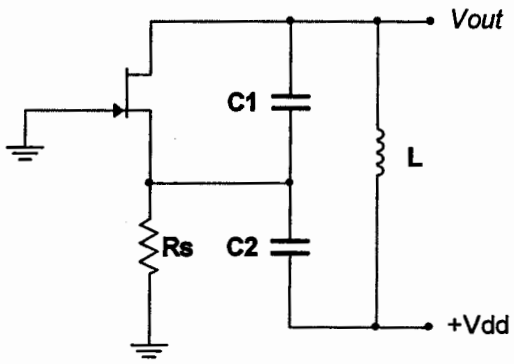
(a) Draw its equivalent circuit and derive expressions for

(i) The oscillating frequency. *(10 marks)*

(ii) The voltage gain required to maintain steady oscillations in the circuit.

(5 marks)

(b) If $C_1 = 100$ pF and $C_2 = 1000$ pF, calculate value of the inductance L and the minimum voltage gain required to maintain steady oscillation at a frequency of 10 MHz.



(5 marks)

Fig. Q3

QUESTION FOUR ***(20 marks)***

a) Define the following terms as used regulated power supplies:

i. Regulation;
ii. Ripple factor;
iii. Peak Inverse Voltage and
iv. Transformer utilization factor.

[4]

b) Prove that:

i. The ripple factor of a half-wave rectified signal is approximately = 1.21
ii. The ripple factor of a full-wave rectified signal is approximately = 0.483

[8]

c) Design a power supply with the following specifications:

Average value of load voltage = 20V;
Maximum value of lead current = 100mA;
With a ripple factor not exceeding 0.01;
Voltage regulation of 2.5%, and
The power line frequency of 50Hz.

[8]

QUESTION FIVE *(20 marks)*

a) The figure 1 below shows a simple series regulator. Describe and explain how this circuit works.

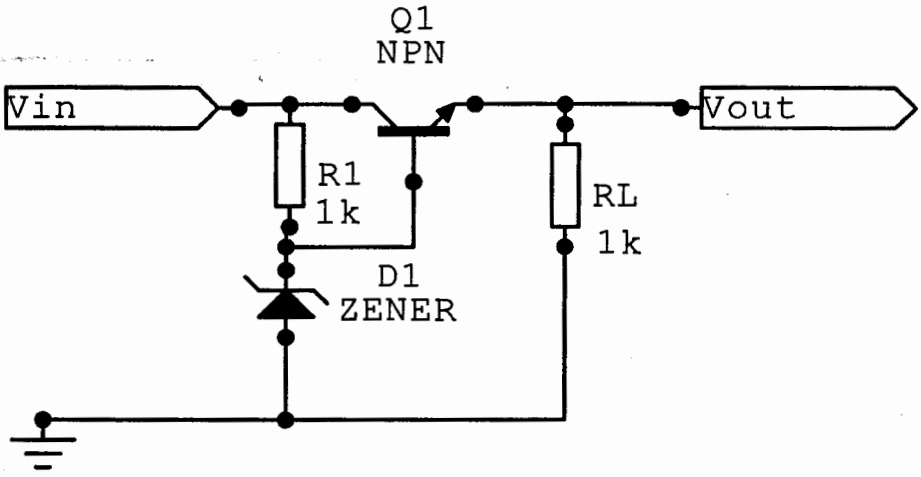


Fig. 1

[6]

b) Design a switching regulator with the following specifications:

Average value of load voltage = 5V;
Average value of lead current = 1A;
Switching frequency at full load = 25 KHz;
Maximum peak to peak ripple should not exceed 0.08V, and
Unregulated supply is = 25V.

[14]

QUESTION SIX ***(20 marks)***

a) With the aid of relevant diagram(s), describe the principles of operation of a binary weighted resistor DAC (digital to analogue converter). Given that a three-bit binary weighted resistor DAC has R = 2 kΩ with a reference voltage of 10V. What would the output voltage be;

(i) if all switches were set to logic 1?.

(ii) if only the least significant bit switch is at logic 1?

[6]

b) With the aid of relevant diagram(s), describe the principles of operation of the R-2R ladder DAC (digital to analogue converter). Given that, the reference voltage is 10V, calculate the output voltage of a three-bit R-2R ladder network if S0 = 1, S1 = 0 and S2 = 1.

[6]

c) With the aid of relevant diagram(s), describe the principles of operation of a three-bit parallel (flash) comparator ADC (analogue to digital converter). Show clearly the encoding tables for the ADC circuit.

[8]