UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, FIRST SEMESTER DECEMBER 2008

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRONIC ENGINEERING

TITLE OF PAPER: ANALOGUE ELECTRONICS III

COURSE CODE: E511

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1.   There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.

2.   Unless otherwise stated, $V_{BE(ON)} = 0.7$ V and $V_T = 0.025$ V.

3.   If you think not enough data has been given in any question you may assume any reasonable values.

4.   A sheet containing some useful equations is attached at the end of this examination paper.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS EIGHT (8) PAGES INCLUDING THIS PAGE

QUESTION ONE   *(25 marks)*

(a)   (i)   Using ± 15 V dual power supplies specify all the circuit components required so that each transistor in the circuits shown in Fig. Q.1a is biased in the active mode with about 1 mA collector current. You can neglect the base currents.   *(8 marks)*

       (ii)   Using your component values predict the quiescent value of V_{CE} in each rransistor.   *(4 marks)*
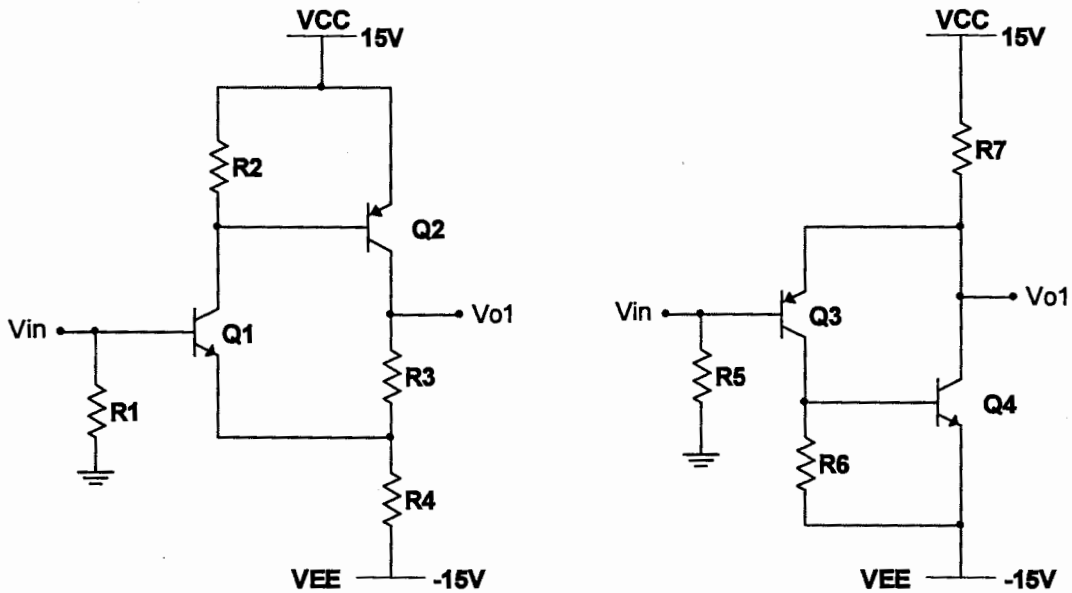

Fiq Q1a

(b)   The circuit in Fig. Q1b operates with dc voltages Vcc and Vi.

       (i)   Derive an equation for the d.c. output voltage V_o in terms of the dc input voltage V_i.

       (ii)   Under what conditions will the transistor Q1 saturate?

       (iii)   By differentiating your expression (i.e. dv_o/dv_i) find the condition under which the circuit is a unity gain inverting amplifier
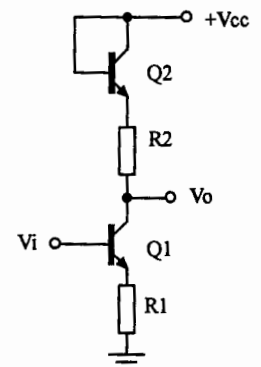
                           (13 marks)

Fig. Q.1b

QUESTION TWO   *(25 marks)*

(a)   (i)   Explain the meaning of base-width modulation in BJTs and show how it may be modeled in BJT circuits.   *(4 marks)*

       (ii)   A BJT has an Early voltage of 150 V and a forward current gain β_F of 75. The BJT operates in the active region with $i_B = 120$ μA. Calculate the output resistance r_o of the BJT.   *(3 marks)*

(b)   The circuit in Fig. Q2b is used as a current source for a differential amplifier.

       (i)   Derive an expression for the small signal output impedance of the current source in terms of the circuit components and BJT device parameters assuming that the BJT has base-width modulation.   *(12 marks)*

       (ii)   If the BJT has $\beta = 100$, $V_A = 100$ V and $R_1 = R_2 = R_E = 2$ kΩ, use your expression to evaluate the output impedance of the current source.   *(6 marks)*
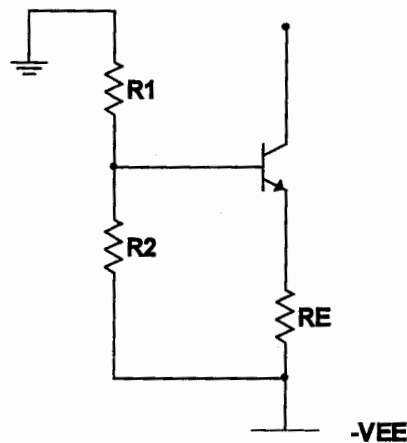
Fig. Q2b

QUESTION THREE   (*25 marks*)

(a)   Given the circuit in Fig. Q3a with $R_{sig} = 1$ kΩ, $R_D = 10$ kΩ, $I = 0.5$ mA, and

$$k_n' \frac{W}{L} = 0.5 \text{ mA/V}^2, \quad V_t = 1 \text{ V}. \text{ Ignore channel-length modulation}$$

     (i)   What overdrive voltage is required to meet these conditions?   *(4 marks)*

     (ii)   What is the input resistance if $V_{ov} = 1.7$V?   *(3 marks)*

     (iii) What is the overall voltage gain?   *(5 marks)*

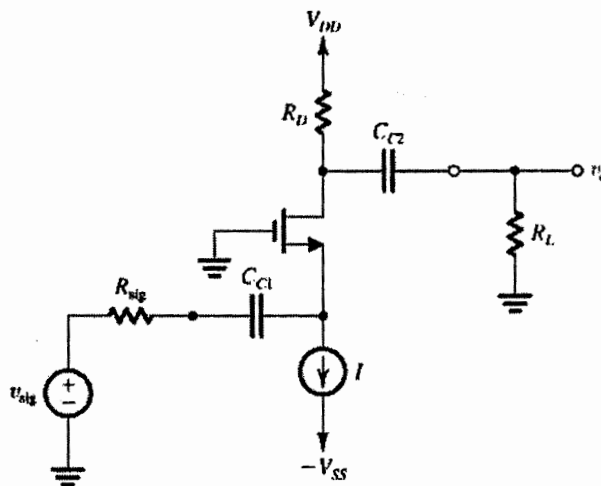**Fig. Q3a**

(b)   The NMOS transistor in the circuit shown in Fig. Q3b has $V_t = 0.9$V and $V_A = 50$ V. If the circuit operates such that $V_D = 2$ V, calculate the small signal voltage gain?   *(5 marks)*
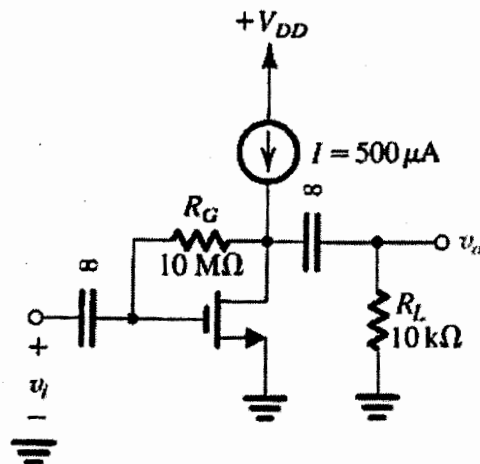

Fig. Q3b

(c)   In the circuit shown in Fig. Q3c, $k_n' \dfrac{W}{L} = 1 \text{ mA/V}^2$ and $V_t = 1 \text{ V}$. Ignore channel

length modulation. What is the the value of the drain voltage ?   (8 marks)

$V_{DD} = +10 \text{ V}$

$R_{G1} = 10 \text{ M}\Omega$

$R_D = 6 \text{ k}\Omega$

$R_{G2} = 10 \text{ M}\Omega$

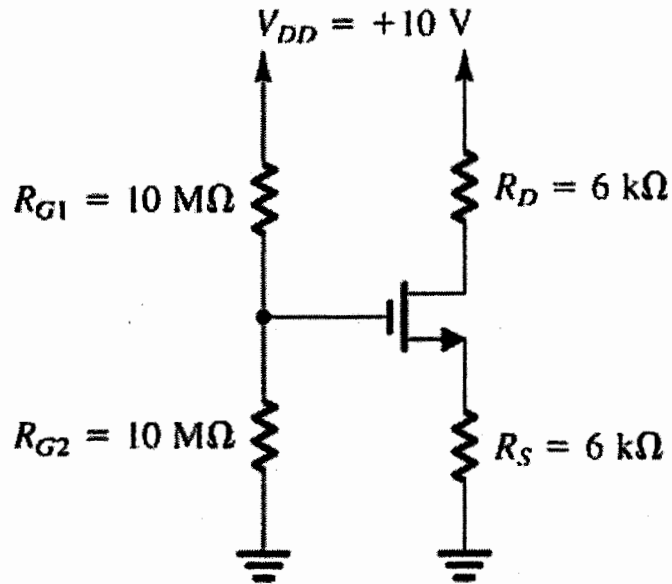$R_S = 6 \text{ k}\Omega$

Fig. Q3c

QUESTION FOUR   *(25 marks)*

(a)   Figure Q4 shows a circuit of an amplifier. Assume that $\beta \gg 1$.

    (i)   Specify a value of R_1 such that $I_{ref} = 2$ mA.

    (ii)   Calculate all branch currents and node voltages. There is no need to redraw the circuit if you do not have time, refer to currents and voltages using the device terminals.   *(15 marks)*
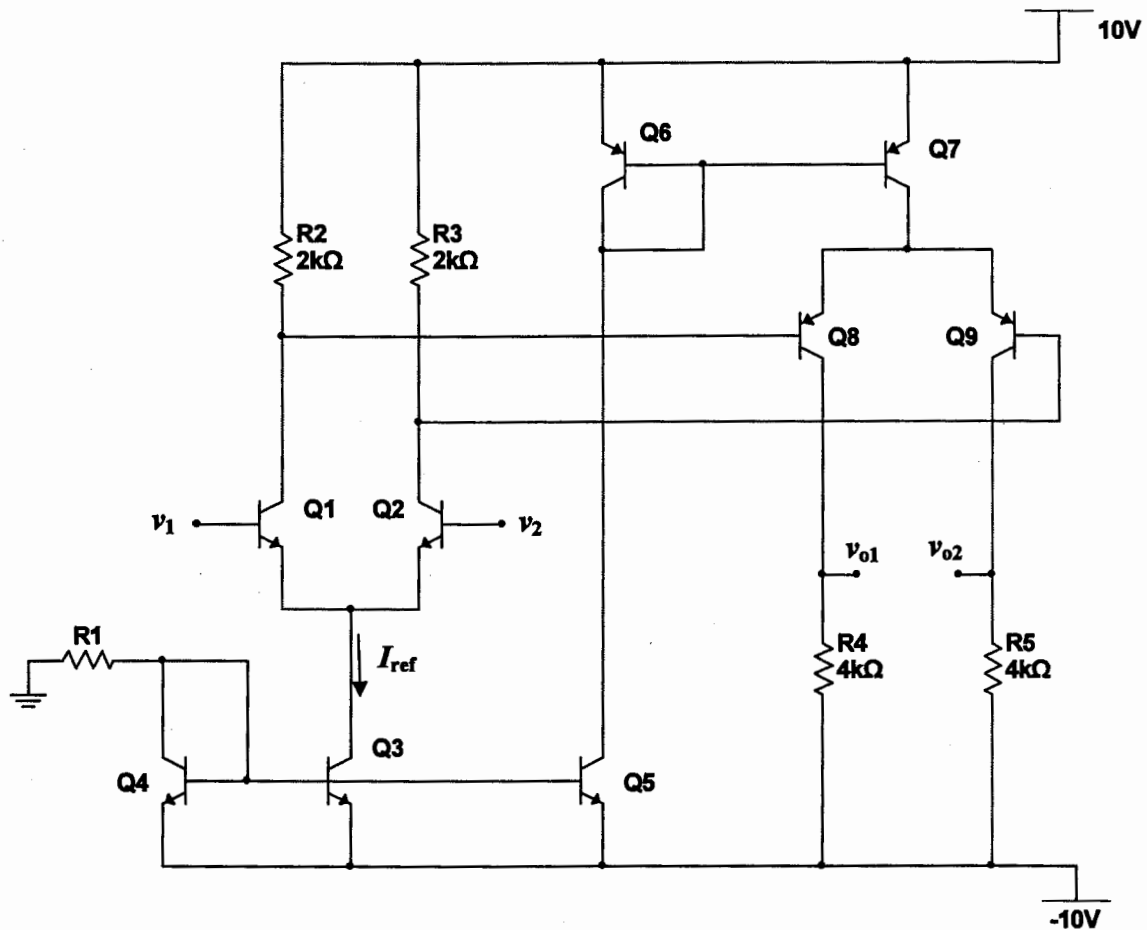

Fig.Q4

(b)   Design a simple current-source biased differential amplifier to give a differential voltage gain of 100 V/V.   *(10 marks)*

QUESTION FIVE *(25 marks)*

(a) For the ciruit shown in Fig.Q5a,

   (i) Use a dc analysis find the power dissipation in the resistor R5 neglecting all base currents. *(10 marks)*

   (ii) Estimate the overall gain of the circuit if $\beta = 100$. Hint first estimate the input and out resistances and gain of each stage. The zener diode may be assumed to have negligible ac resistance and $V_A = \infty$. *(10 marks)*
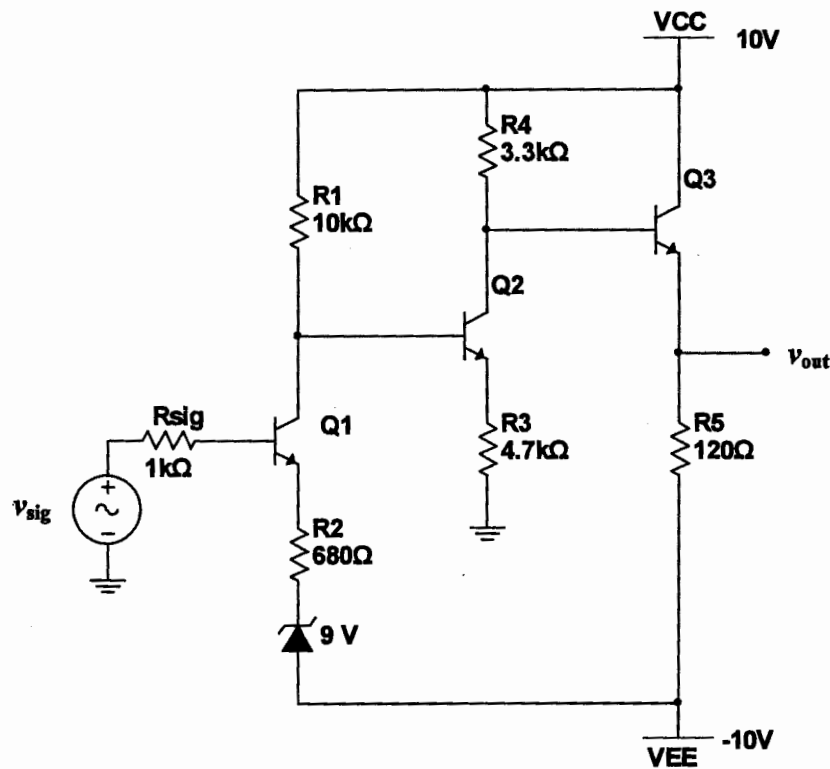

Fig.Q5a

(b) Draw a CMOS logic circuit which implements the logic function $Y = \overline{A} + B(\overline{C} + D)$. How many transistors are needed to implement the function? *(5 marks)*

SOME USEFUL MOSFET EQUATIONS

$$i_D = k_n' \frac{W}{L}\left[(v_{GS}-V_t)v_{DS}-\frac{1}{2}v_{DS}^2\right] \text{ in triode region}$$

$$i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2 \text{ in saturation region}$$

$$i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS}) \text{ in saturation region with Channel Modulation effect}$$

BJT EBERS-MOLL EQUATIONS

$$i_E = \frac{I_s}{\alpha_F}\left(e^{v_{BE}/V_T}-1\right)-I_s\left(e^{v_{BC}/V_T}-1\right)$$

$$i_C = I_s\left(e^{v_{BE}/V_T}-1\right)-\frac{I_s}{\alpha_R}\left(e^{v_{BC}/V_T}-1\right)$$

$$i_B = \frac{I_s}{\beta_F}\left(e^{v_{BE}/V_T}-1\right)+\frac{I_s}{\beta_R}\left(e^{v_{BC}/V_T}-1\right)$$