UNIVERSITY OF SWAZILAND

SUPPLEMENTARY EXAMINATION, JULY 2009

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER: ANALOGUE ELECTRONICS III

COURSE CODE: E511

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. **There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.**
2. **Unless otherwise stated, $V_{BE(ON)} = 0.7$ V and $V_T = 0.025$ V.**
3. **If you think not enough data has been given in any question you may assume any reasonable values.**
4. **A sheet containing some useful equations is attached at the end of this examination paper.**

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

(a) (i) Explain what is meant by the "Early Effect" in BJTs and show how it may be modeled in BJT circuits. *(5 marks)*

(ii) A BJT has an Early voltage of 100 V and a forward current gain β_F of 100. The BJT operates in the active region with $i_B = 80\ \mu A$. Calculate the transconductance g_m and output resistance r_o of the BJT. *(5 marks)*

(b) In what mode is the BJT in Fig.Q.1b operating? Justify your answer. *(5 marks)*

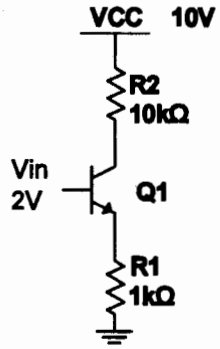

Fig. Q.1b

(c) Explain the operation of the circuit in Fig.Q.1c. *(5 marks)*

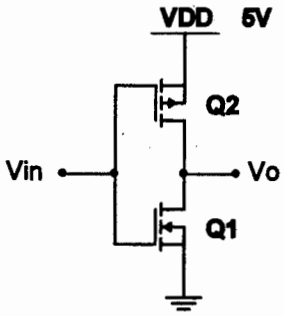

Fig. Q.1c

(d) Calculate the current I in the circuit shown in Fig.Q.1d. *(5 marks)*

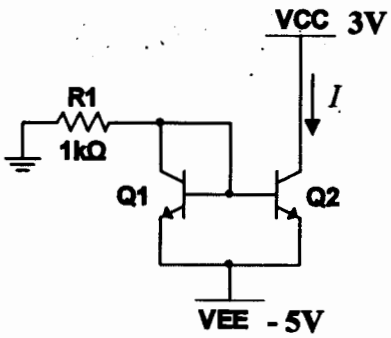

Fig. Q.1d

QUESTION TWO ***(25 marks)***

(a) Draw a CMOS logic circuit which implements the logic function $\mathbf{Y = \overline{AB} + \overline{C}\,\overline{D}}$.

How many transistors are needed to implement the function? *(9 marks)*

(b) A MOSFET with $k_n' \frac{W}{L} = 0.5$ mA/V^2 and $V_t = 2.5$ V is connected as shown in Fig.Q2b. In what region is the transistor operating when:

(i) R = 2.0 kΩ, and

(ii) R = 0.5 kΩ?

Justify your answer in each case. *(10 marks)*

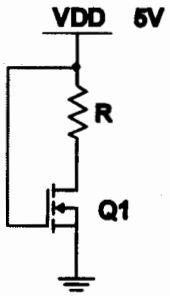

Fig.Q.2b

(c) An NMOS with $k_n' \frac{W}{L} = 3.0$ mA/V^2 and $V_t = 0.5$ V is connected as shown in Fig.Q1c.

Obtain the value of input voltage V_{in} when it crosses from the triode region of operation to the saturation region. *(6 marks)*

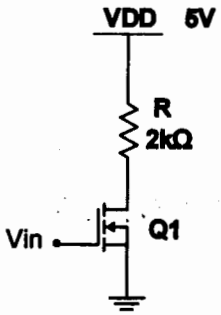

Fig.Q.2c

QUESTION THREE ***(25 marks)***

(a) Design a Widlar current source as shown in Fig.Q3a to give an output current I_o of 20 μA. You are to use resistors of values not greater than 10 kΩ. For the transistors assume that $V_{BE} = 0.7$ V at 1 mA and neglect the effect of finite β.

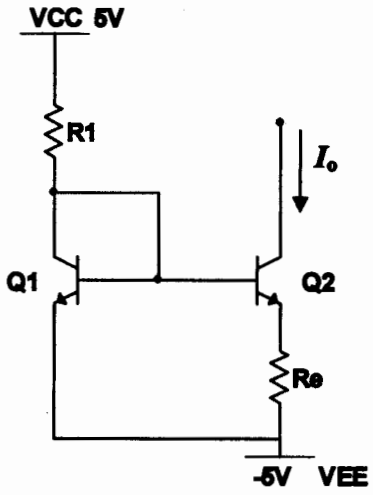

Fig. Q.3a

(b) Determine the output current at $V_o = 5$ V for the MOS current mirror given in Fig.Q.3b. You are given that $I_{ref} = 4$ mA and the transistors used have :

$V_{t1} = V_{t2} = 1$ V,

$\lambda_1 = 0$, $\lambda_2 = 0.02$ V^{-1}, and

$k_n'\left(\frac{W}{L}\right)_1 = 200$ μA/V^2, $k_n'\left(\frac{W}{L}\right)_2 = 300$ μA/V^2

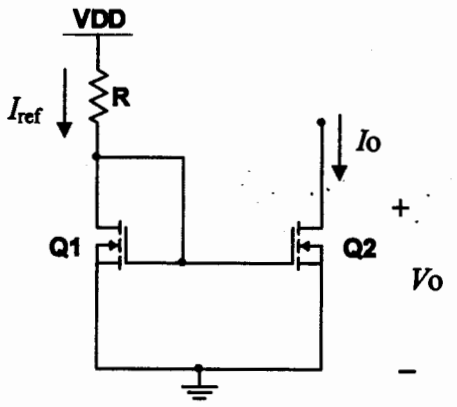

Fig. Q.3b

QUESTION FOUR ***(25 marks)***

A basic differential amplifier circuit is shown in Fig.Q4. Assume that the transistor are matched with β=100 and that the Early Effect is negligible in Q1 and Q2, except in Q3 where V_A = 100 V. For small signal inputs, calculate:

(a) the single-ended gain to a differential input. *(7 marks)*

(b) the differential gain to a differential input *(2 marks)*

(c) the differential input resistance *(4 marks)*

(d) the common-mode gain to a single-ended output. *(5 marks)*

(e) the common-mode gain to a differential output. *(2 marks)*

(f) the Common-Mode Rejection Ratio. *(5 marks)*

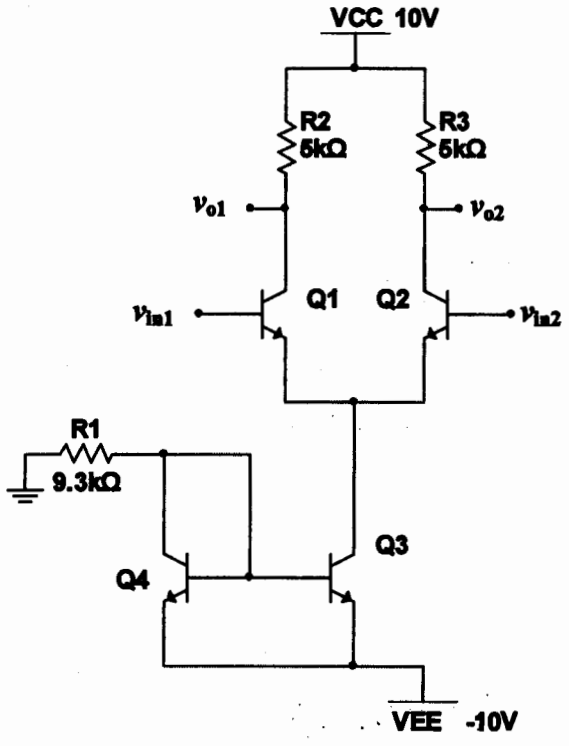

Fig.Q4

QUESTION FIVE *(25 marks)*

For the circuit shown in Fig.Q.5 ,

$\mu_n C_{ox} = 2\ \mu A/V^2$, $\mu_p C_{ox} = 18\ \mu A/V^2$, $(W/L)_n = (W/L)_p = 3$, and $|V_{tn}| = |V_{tp}| = 1V$

Find the current I_D and voltage V_o. *(25 marks)*

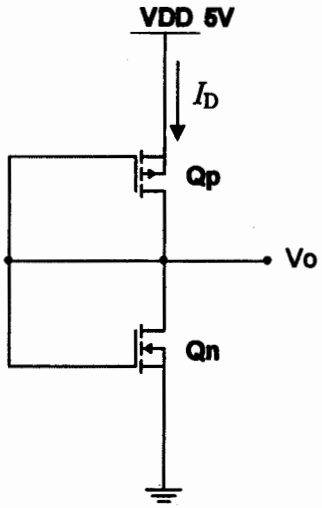

Fig.Q5