UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, SECOND SEMESTER MAY 2009

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE ELECTRONICS IV
COURSE CODE:	E512
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. There are six questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. Unless otherwise stated, $V_{BE(ON)} = 0.7$ V and $V_T = 0.025$ V.
3. If you think not enough data has been given in any question you may assume any reasonable values.
4. A sheet containing some useful equations is attached at the end of this examination paper.
5. Calculators capable of doing multiplication and division of complex numbers may be used.

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THIS PAPER CONTAINS EIGHT (8) PAGES INCLUDING THIS PAGE

QUESTION ONE ***(25 marks)***

(a) Briefly discuss the requirements for a good quality power output stage. *(7 marks)*

(b) For the power output stage shown in Fig.Q1 assume that $I = 100$ mA, $V_{CEsat} = 0.3$ V and $V_{cc} = 15$ V.

(i) For a load resistance R_L of 120 Ω, determine the maximum undistorted input signal that can be applied to the input and calculate the power conversion efficiency under this condition. Note that the power dissipation in Q3 and R is not negligible. *(10 marks)*

(ii) Determine a value of R_L which gives maximum efficiency. *(4 marks)*

(iii) Hence evaluate the maximum efficiency of the circuit. *(4 marks)*

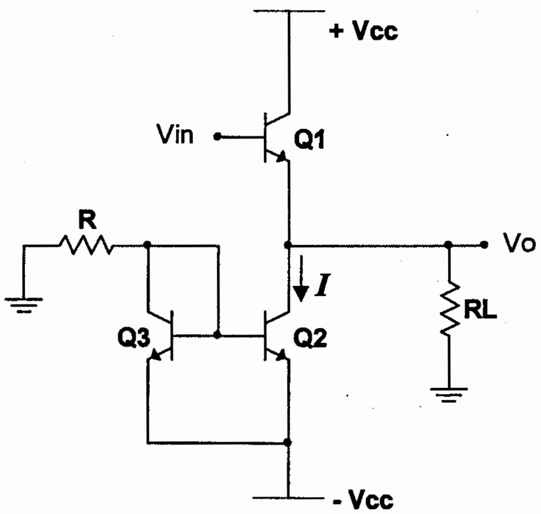

Fig Q1

QUESTION TWO ***(25 marks)***

You are required to design the biasing circuit for the class AB output stage shown in Fig. Q2. The following relevant data are given:

$I_{C1} = I_{C2} = 0.6$ mA under quiescent conditions.

Q_1, Q_2, Q_3 and Q_4 are similar but Q_1, Q_2 have 3 times the junction areas of Q_3, Q_4.

$I_S = 10^{-12}$ mA for Q_3, Q_4.

Vcc = 20 V.

Maximum load current = 20 mA.

Find:

(a) The required current in Q_3 and Q_4. *(5 marks)*

(b) Determine suitable values of R1 and R2 that ensure that all transistors are always operating in the active region. You must verify the validity of your values under all worst case conditions. *(15 marks)*

(c) Find the quiescent power dissipation all the transistors in the circuit. *(5 marks)*

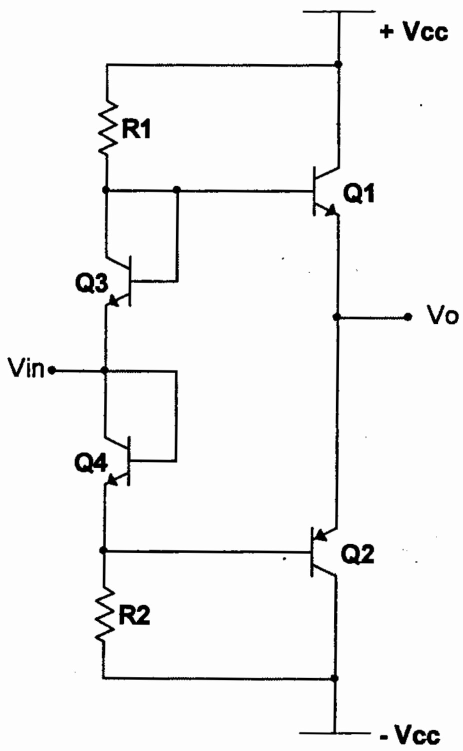

Fig. Q2

QUESTION THREE ***(25 marks)***

(a) With the aid of a suitable illustration briefly discuss the factors which limit the safe operating area of a bipolar junction power transistor. *(5 marks)*

(b) A BJT with a maximum junction temperature of 175°C and thermal resistance θ_{JC} = 2.5°C/W is bonded to a washer of thermal resistance θ_{JC} = 0.45°C/W. The transistor is then fixed to a heat sink of θ_{SA} = 1°C/W per cm length. Determine the length of heat sink required for the transistor to safely dissipate 40 W of power at an ambient temperature of 40°C? *(6 marks)*

(c) The full power rating of 100 W for a given transistor is available up to 25°C and its maximum junction temperature is 150°C.

(i) Estimate its thermal resistance. *(2 marks)*

(ii) What maximum power would you allow the device to dissipate without a heat sink at an ambient temperature of 60°C. *(2 marks)*

(iii) State any assumptions you have made in your calculations. *(1 mark)*

(d) Two possible amplifier configurations are shown in Fig. Q.3d.

(i) Show that both of them have equal signal gains. *(5 marks)*

(ii) Compare their noise performances and comment on the practical implications of the better one of the two. *(4 marks)*

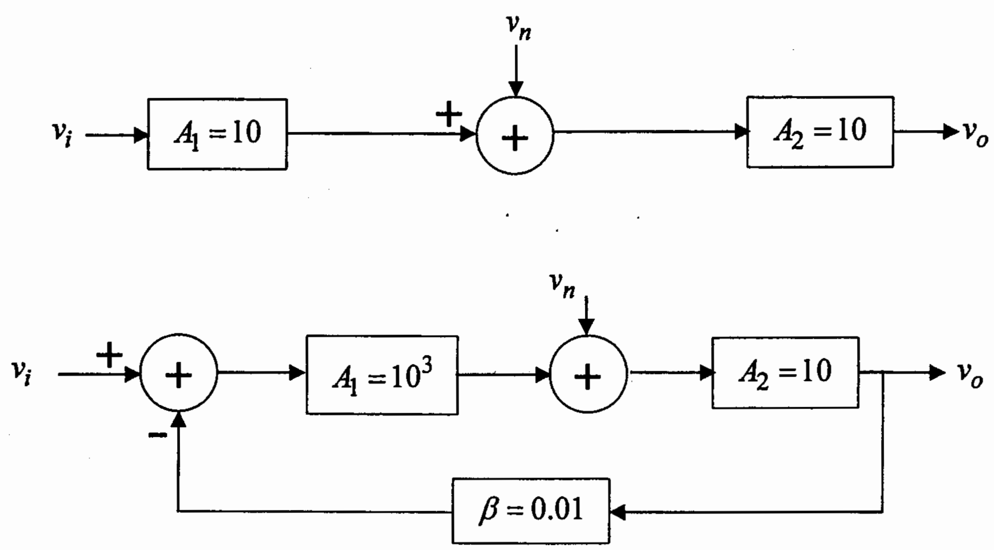

Fig. Q3d

QUESTION FOUR ***(25 marks)***

(a) Determine the components of a lossless L-section to match a 50 Ω source to a 75 Ω load at 400 MHz. *(7 marks)*

(b) A 50-Ω source is to be matched to a high frequency amplifier whose input admittance at 500 MHz is $8 - j12$ mS. Determine the components of a lumped L-section network suitable for the match. A Smith Chart may be used. *(18 marks)*

QUESTION FIVE ***(25 marks)***

The 2N5943 transistor biased at $V_{CE} = 15$ V and Ic = 5 mA has the following common emitter y-parameters at 300 MHz:

$$y_{11} = 25.34 + j7.05 \text{ mS}$$
$$y_{12} = 0.035 - j3.952 \text{ mS}$$
$$y_{21} = 4.378 - j142.3 \text{ mS}$$
$$y_{22} = 1.321 + j11.452 \text{ mS}$$

(a) Determine whether the transistor is unconditionally stable or not under these bias conditions and frequency. *(5 marks)*

(b) What maximum possible power gain obtainable from this transistor at these bias conditions and frequency? *(5 marks)*

(c) If the device is fed from a 50-Ω source and the load is 75 Ω, determine:

(i) Whether the circuit is stable under these conditions. *(5 marks)*

(ii) The expected voltage gain. *(5 marks)*

(iii) The input admittance of the circuit. *(5 marks)*

QUESTION SIX ***(25 marks)***

Consider the circuit of a boost converter is shown in Fig. Q6.

(a) With the aid of appropriate sketches explain the operation of the circuit. *(9 marks)*

(b) Calculate the output voltage expected. *(2 marks)*

(c) Calculate the average value of the load current. *(2 marks)*

(d) Calculate the power delivered to the load. *(2 marks)*

(e) Find the supply current. *(2 marks)*

(f) Determine the minimum and maximum values of the inductor current. *(8 marks)*

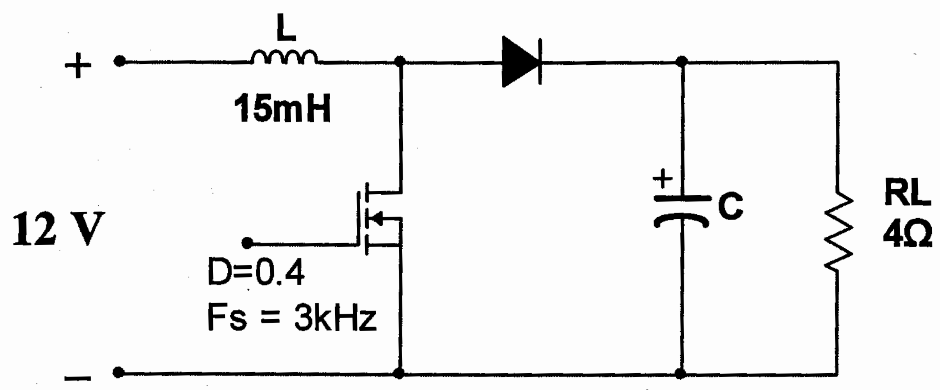

Fig. Q6

SOME RF CIRCUIT DESIGN EQUATIONS

$$C = \frac{|y_f y_r|}{2g_i g_o - \mathrm{Re}(y_f y_r)}$$

$$MAG = \frac{|y_f y_r|^2}{4g_i g_o}$$

$$K = \frac{2(g_i + G_S)(g_o + G_L)}{|y_f y_r| + \mathrm{Re}(y_f y_r)}$$

$$1 + Q^2 = \frac{R_p}{R_s} \quad \text{where} \quad Q = \frac{R_p}{X_p} = \frac{X_s}{R_s}$$