UNIVERSITY OF SWAZILAND

SUPPLEMENTARY EXAMINATION, JULY 2009

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER: ANALOGUE ELECTRONICS IV

COURSE CODE: E512

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. **There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.**
2. **Unless otherwise stated, $V_{BE(ON)} = 0.7$ V and $V_T = 0.025$ V.**
3. **If you think not enough data has been given in any question you may assume any reasonable values.**
4. **A sheet containing some useful equations is attached at the end of this examination paper.**
5. **Smith Charts which may be used to solve some problems are attached.**

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS EIGHT (8) PAGES INCLUDING THIS PAGE

QUESTION ONE ***(25 marks)***

(a) At an ambient temperature $T_A = 25°C$, a BJT is specified to have a maximum power dissipation P_{Dmax} of 20 W and a maximum junction temperature T_{Jmax} of 150°C. Find the following:

(i) The thermal resistance θ_{JA} of the BJT. *(3 marks)*

(ii) The maximum power that it can safely dissipate at an ambient temperature of 50°C. *(3 marks)*

(iii) The junction temperature when the device is dissipating 10 W at an ambient temperature of 25°C. *(3 marks)*

(b) Consider the calss AB output stage using a V_{BE} multiplier as shown in Fig Q.1b. In this circuit $V_{cc} = 15$ V, $R_L = 100\ \Omega$, and the output V_o is sinusoidal with a maximum amplitude of 10 V. Let Q_N and Q_P be matched with $I_S = 10^{-13}$ A and $\beta = 50$.

(i) Suggest with justification a suitable value for the bias current I_{bias} for the circuit to work properly. *(4 marks)*

(ii) For a quiescent current of $I_Q = 2$ mA in the output transistors, what bias voltage should the V_{BE} multiplier provide? *(5 marks)*

(iii) If the V_{BE} multiplier transistor Q_1 has $I_S = 10^{-14}$ A and a large β, complete the design by specifying the values of R_1 and R_2 that would result in the bias voltage you worked out in (ii). *(7 marks)*

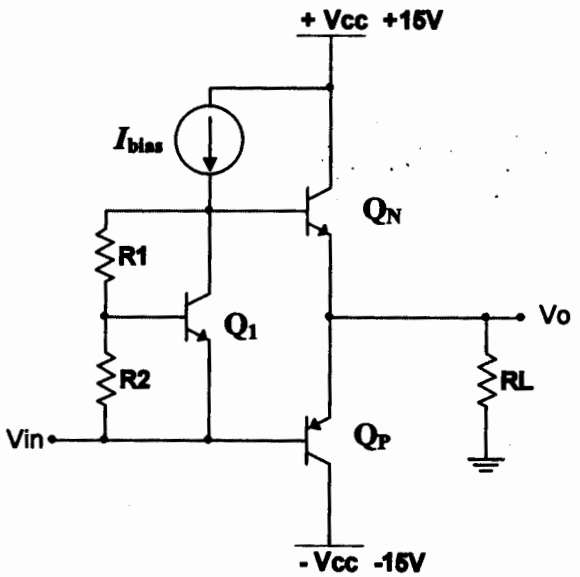

Fig.Q.1b

QUESTION TWO ***(25 marks)***

(a) A 12V battery V_2 is being charged using a 30 V source V_1 through an inductor in a switching mode as shown in Fig.Q.2a. The switch is operating at 1 kHz with a duty cycle of 0.4. The inductor is designed to make the charging current smooth with a tolerable ripple. What value of inductor will limit the peak-to-peak current to 100 mA? *(5 marks)*

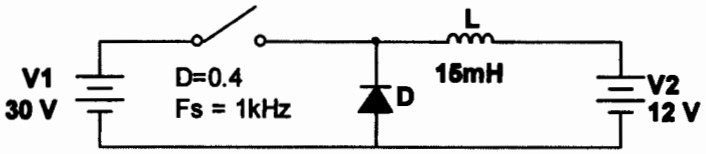

Fig.Q.2a

(b) For the emitter follower power amplifier stage shown in Fig.Q.2b. with ±9 V supplies and BJTs with high β, find a value of R which would give a design capable of ±7 V outputs with a 1-kΩ load R_L. *(5 marks)*

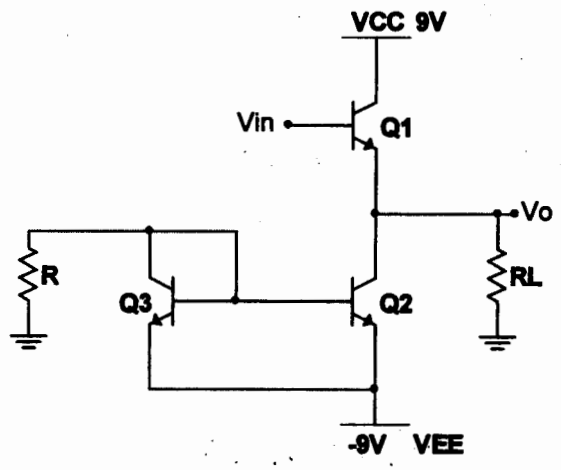

Fig.Q.2b

(c) For the class B complementary stage shown in Fig.Q.2c with ±10 V supplies and a 100-Ω load R_L, assume that $V_{CEsat} = 0.3$ V and $V_{BE} = 0.7$ V. Calculate the following:

(i) The maximum sinewave output power available. *(5 marks)*

(ii) The maximum input signal. *(2 marks)*

Question 2(c) Continued ...

(iii) The average power dissipation of each BJT. *(5 marks)*

(iv) The maximum efficiency of the stage. *(3 marks)*

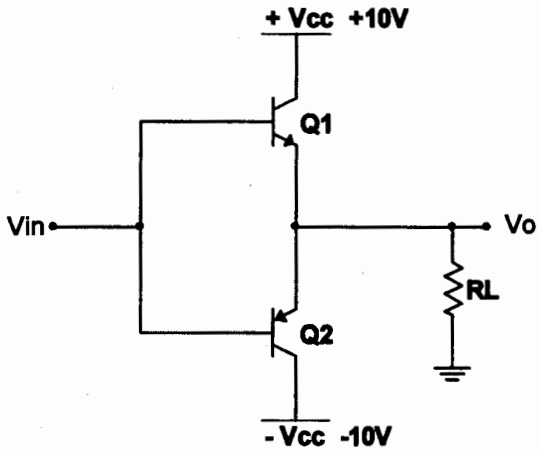

Fig.Q.2c

QUESTION THREE ***(25 marks)***

The amplifier whose schematic is shown in Fig.Q.3 is dc coupled throughout and is biased using the three current sources shown. The n-type transistors are matched with $\beta_N = 100$, and the p-type transistors are also matched with $\beta_P = 75$. By performing step-by-step dc analysis of each stage of the amplifier, determine the output voltage V_o appearing across a load resistance R_L of 1 kΩ. Note that dc coupled stages interact and base currents are not negligible for all the transistors. *(25 marks)*

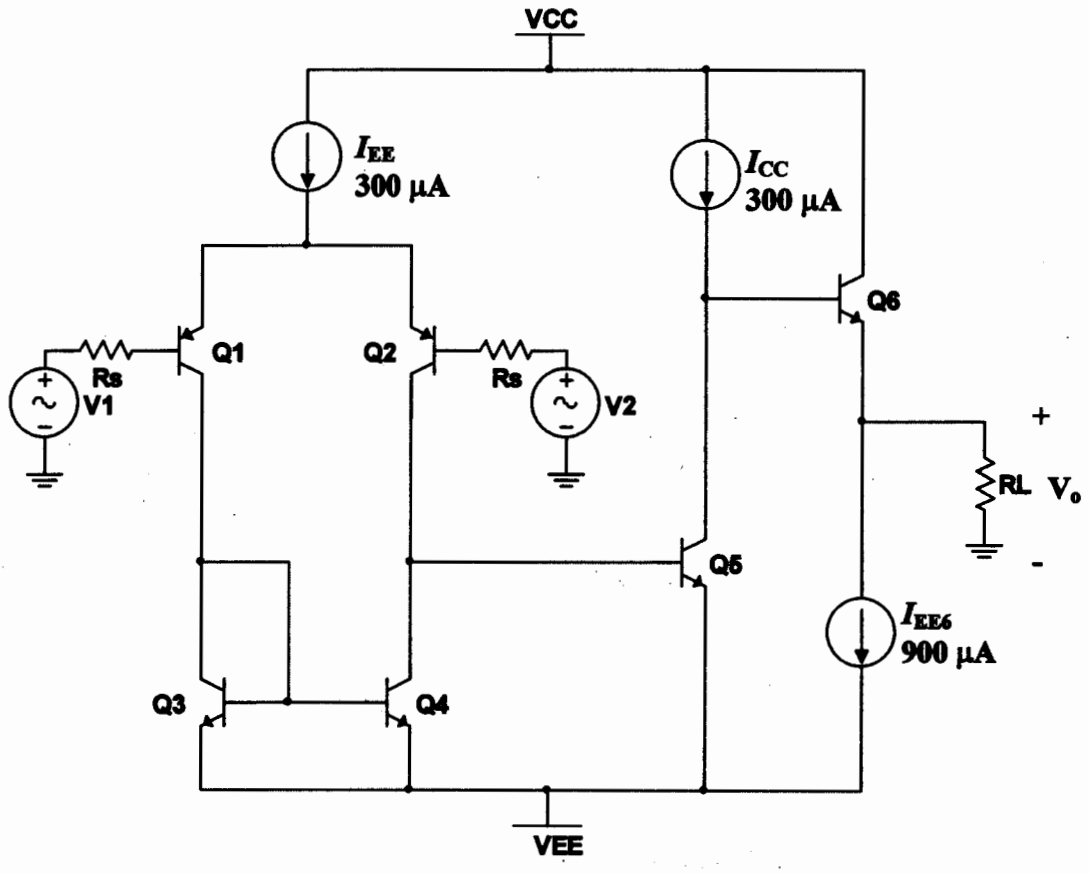

Fig.Q.3

QUESTION FOUR ***(25 marks)***

(a) A signal source has a signal-to-noise ratio of 20 dB and produces signal power of 50μW to a matched load. The signal from the source is amplified by a matched amplifier whose gain is 35 dB. The amplifier itself produces noise of 200 nW referred to its input. Calculate:

(i) The noise power in the source. *(4 marks)*

(ii) The noise figure of the amplifier. *(6 marks)*

(b) Determine and sketch the components of an L-section matching network for matching a 75 Ω source to a load of 300 Ω at a frequency of 100 MHz.

(15 marks)

QUESTION FIVE ***(25 marks)***

A transistor 2N5179 at $V_{CE} = 6.0$ V, $I_C = 1.5$ A has the following y-parameters at 300 MHz:

$$y_{11} = 4.8 + j9.6 \text{ mS}$$
$$y_{12} = -0.09 - j1.15 \text{ mS}$$
$$y_{21} = 36.5 - j26.8 \text{ mS}$$
$$y_{22} = 0.42 + j2.65 \text{ mS}$$

(a) Examine the stability of the device at this bias point and frequency. Is the device usable? Explain your answer. *(8 marks)*

(b) Up to what power amplification would you expect the device to give under ideal conditions? *(5 marks)*

(c) The device is driven from from a source of 70 Ω and feeds into a 100 Ω load. Draw the y-parameter equivalent circuit and calculate the voltage gain of the circuit. *(12 marks)*