UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, FIRST SEMESTER DECEMBER 2009

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER: ANALOGUE ELECTRONICS III

COURSE CODE: E511

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. **There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.**
2. **If you think not enough data has been given in any question you may assume any reasonable values.**
3. **A sheet containing some useful equations is attached at the end of this examination paper.**

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE ***(25 marks)***

(a) The LED in Fig.Q.1a has a forward voltage V_D = 1.8 V and requires at least 2 mA of current to achieve proper brightness. The LED is rated at 20 mW. Choose R_B and R_C for reliable illumination if the BJT has $\beta \geq 60$, V_{CEsat} = 0.3 V and V_{in} to switch on is 6 V. ***(9 marks)***

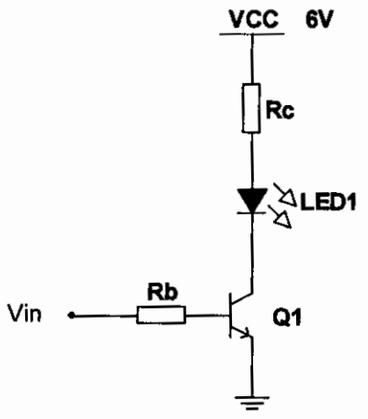

Fig Q.1a

(b) For the circuit shown in Fig.Q.1b assume that all the transistors have β = 100. Calculate the voltages at all the nodes of the circuit. ***(16 marks)***

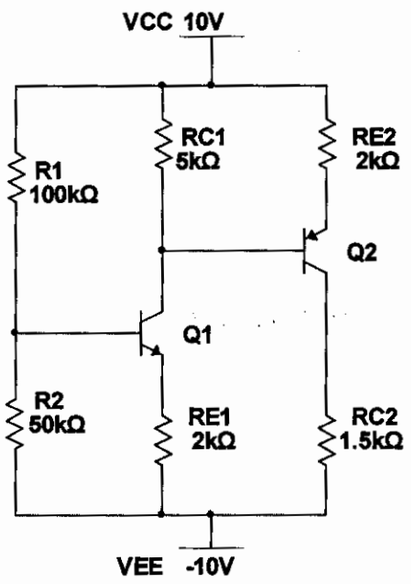

Fig Q.1b

QUESTION TWO (25 marks)

(a) An NMOS transistor has V_{DS} = 3.3 V, W = 10 μm, L = 1 μm, V_t = 0.7 V and $k_n' = 25\ \mu A/V^2$.

(i) Calculate the transconductance for V_{GS} = 2 V and 3.3 V. ***(4 marks)***

(ii) Check the saturation region assumption for both cases. ***(2 marks)***

(b) The transistor given in Q.2a is used in the circuit shown in Fig. Q.2b with the added information that $\lambda = 0.025\ V^{-1}$. Calculate the drain current. ***(9 marks)***

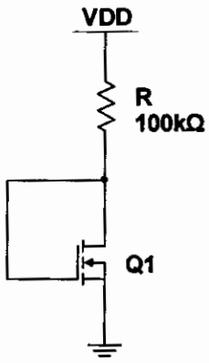

Fig Q.2b

(c) An NMOS transistor is used as a switch which must conduct I_D = 4 A with $V_{DS} \leq 0.1$ V. when it is on. If the gate to source voltage to turn it on is 5 V and V_t = 2 V, what value of transconductance parameter $k_n' \frac{W}{L}$ is required to implement the switch?

(10marks)

QUESTION THREE ***(25 marks)***

Consider the circuit given in Fig.Q.3. The MOSFET has $k_n' \frac{W}{L} = 0.25$ mA/V^2 and $V_t = 2$ V.

(a) Explain why the resistor R_G guarantees that the transistor is biased in the saturation region. ***(3 marks)***

(b) Find the value of R_D which establishes a drain current of 2 mA. ***(5 marks)***

(c) Calculate the voltage gain of the circuit assuming that $\lambda = \infty$. ***(6 marks)***

(d) Calculate the input resistance of the circuit. ***(5 marks)***

(e) Find the largest allowable a.c. input signal swing if the transistor is to remain in the saturation region. Check that the MOSFET remains conducting in the saturation region at both extremes of the voltage swing. ***(6 marks)***

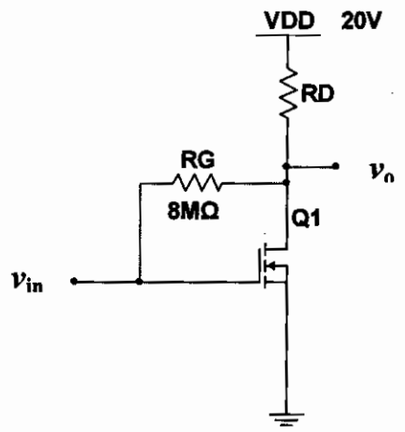

Fig.Q3

QUESTION FOUR ***(25 marks)***

(a) An unusual current mirror circuit is shown in Fig.Q.4a. The transistors may be assumed to be matched and the base currents may be assumed to be negligible compared with collector currents.

(i) Obtain an expression relating I_{ref} and I_o. ***(7 marks)***

(ii) Use your relation to show that $I_o \geq I_{ref}$. ***(2 marks)***

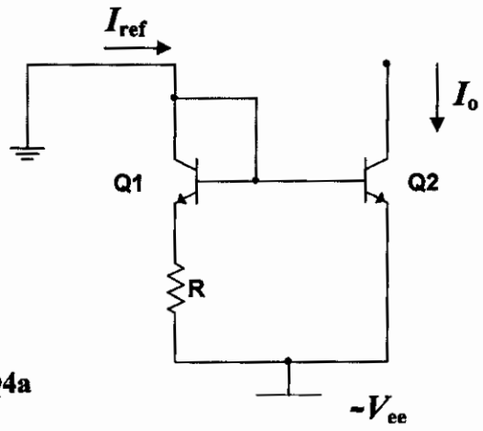

Fig.Q4a

(b) In the circuit of Fig.Q.4b, the transistor parameters are:

For NPN: $\beta_N = 150$, $V_{AN} = 100\,\text{V}$ and **for PNP:** $\beta_P = 50$, $V_{AP} = 75\,\text{V}$

(i) Find the value of R necessary to establish a quiescent (dc bias) collector current, I_{C1}, of 1 mA in Q1. Remember base currents are not negligible. ***(4 marks)***

(ii) Calculate the gain, v_o / v_s, of the circuit. ***(12 marks)***

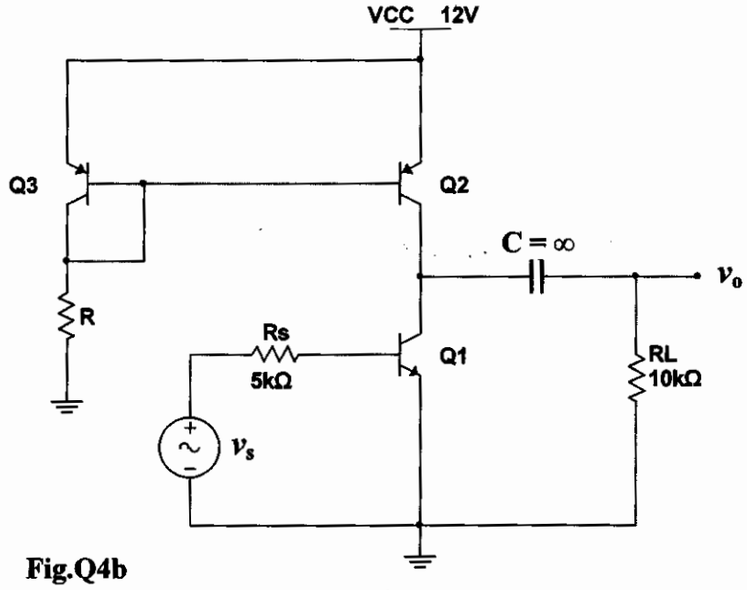

Fig.Q4b

QUESTION FIVE ***(25 marks)***

A two-stage CMOS amplifier is shown in Fig.Q.5. You are required to determine an expression for the mid-band gain $v_o/(v_1 - v_2)$ in terms of the circuit bias current I. The parts of the question below give you one way in which you can arrive at the required final expression. You may however follow any other way if you wish for full marks if you get it correct. The figures next to each MOSFET indicate its aspect ratio W/L.

For PMOS: $k_p' = 20\ \mu\text{A/V}^2,\ \lambda_p = 0.02\,\text{V}^{-1}$

For NMOS: $k_n' = 20\ \mu\text{A/V}^2,\ \lambda_n = 0.01\,\text{V}^{-1}$

(a) Obtain the drain currents in Q5 and Q8 in terms of I.

(b) Obtain the differential gain of Q5, Q1, Q2, Q3, Q4 differential amplifier in terms of I.

(c) Obtain the gain of the Q7 and Q8 second stage.

(d) Obtain the overall gain. In terms of I.

Comment on the usefulness of I in the circuit.

(25 marks)

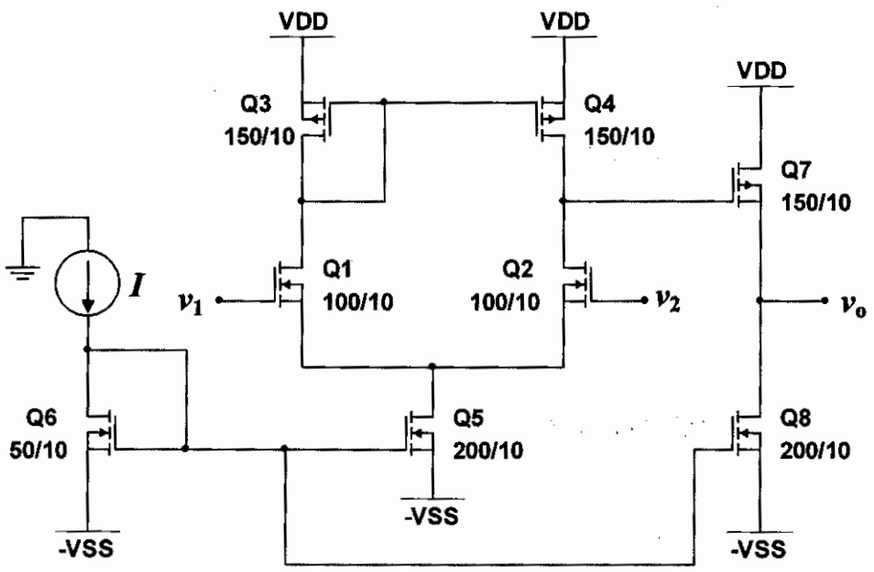

Fig.Q.5

1. SOME USEFUL MOSFET EQUATIONS

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \text{ in triode region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \text{ in saturation region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \text{ in saturation region with Channel Modulation effect}$$

$$V_A = 1/\lambda$$

2. BJT EBERS-MOLL EQUATIONS

$$i_E = \frac{I_s}{\alpha_F}\left(e^{v_{BE}/V_T} - 1\right) - I_s\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_C = I_s\left(e^{v_{BE}/V_T} - 1\right) - \frac{I_s}{\alpha_R}\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_B = \frac{I_s}{\beta_F}\left(e^{v_{BE}/V_T} - 1\right) + \frac{I_s}{\beta_R}\left(e^{v_{BC}/V_T} - 1\right)$$

3. Unless otherwise stated, $V_{BE(ON)} = 0.7$ V and $V_T = 0.025$ V.