UNVERSITY OF SWAZILAND

MAIN EXAMINATION – SEMESTER I NOV/DEC 2010

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF THE PAPER: ANALOG ELECTRONICS III

COURSE CODE: E511

TIME ALLOWED: 3 HOURS

INSTRUCTIONS:

1. **THERE ARE SIX QUESTIONS IN THIS PAPER. ANWSER ANY FIVE OF THEM. EACH QUESTION CARRIES 20 MARKS**
2. **IF YOU THINK NOT ENOUGH DATA HAS BEEN GIVEN IN THE QUESTION YOU MAY ASSUME ANY REASONABLE VALUES.**

THIS PAPER SHOULD NOT BE OPE UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SIX PAGES INCLUDING THIS PAGE.

Q 1

A) What is the tunneling phenomenon? Draw the I-V characteristics and energy band diagrams of a tunnel diode. Mention some applications of a tunnel diode.

10 Marks

B) Discuss Opto couplers and isolators. What are they used for in practice?

6 marks

C) What is the significance of CMRR in opamps? An opamp has a CMRR of 1000. One set of signals v_1 = +60 μV, v_2 = -60 μV and another set v_1 = 1060 μV, v_2 = 940 μV are applied separately to its input. By what factor does the output voltage change for the two sets of input signals? **4** Marks

Q 2

A) A MOSFET has a drain circuit resistance R_d = 100 kΩ and operates at 25 kHz. Calculate the voltage gain of this device as a single stage and then as the first transistor in a cascade consisting of two identical stages and determine the value of C_i. The MOSFET parameters are:

g_m = 1.6 mA/V, r_d = 45 kΩ, C_{gs} =3.0 pF, C_{ds} =1.0 pF, and C_{gd} = 2.8pF.

14 marks

B) The amplifier of Fig. 2B, utilizes an n-channel FET for which Vp = -2 V and I_{DSS} = 1.7 mA. It is required to bias the circuit at I_D= 0.9 mA, using Vdd=24 V. Assume $r_D \geq$ Rd. Find Vgs, gm, Rs, and Rd, such that the voltages gain is at least 20 db, with Rs bypassed with a very large capacitance Cs.

6 marks

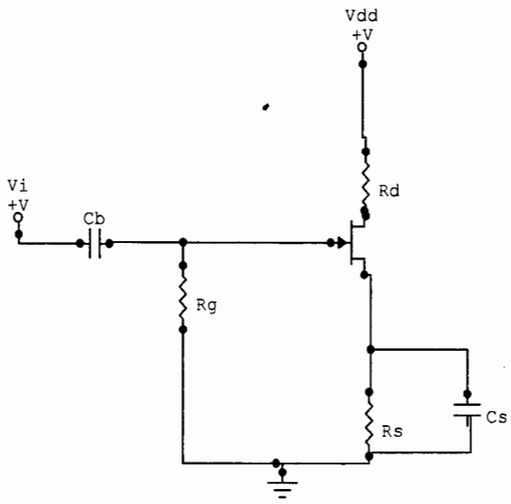

Figure 2 B Source self bias circuit

Q 3

A) Name the two basic types of photodetector diodes. With the aid of a suitable diagram explain the operation of any one of them. ***4*** marks

B) Determine the cutoff frequency and wavelength for InGaAsP, given that photon energy $E_{ph} = E_g = 0.89$ eV, and Plank's constant $h = 6.626 \times 10^{-34}$. ***4*** marks

C) Sketch the circuit diagrams of CMOS and TTL NAND and NOR logic gates and explain their operation. **7** marks

D) For the circuit shown in Fig. Q.3D derive, giving explanations, the Boolean expression for the output Q in terms of the logic inputs variables X_1 and X_2. **5** marks

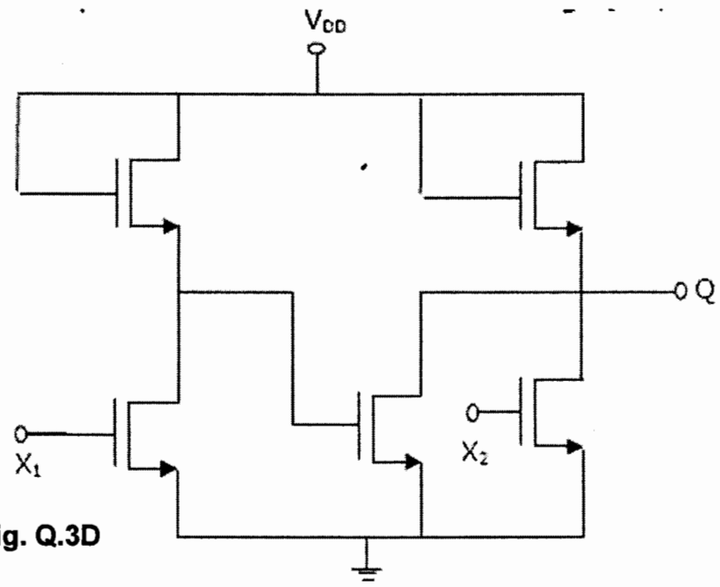

Fig. Q.3D

Q 4

A) For the circuit of Fig. Q4 A determine the value of resistance R2 to provide constant current I=10 mA in the load, when Vz=6V and supply voltage V = 12 V and give some applications. **6** marks

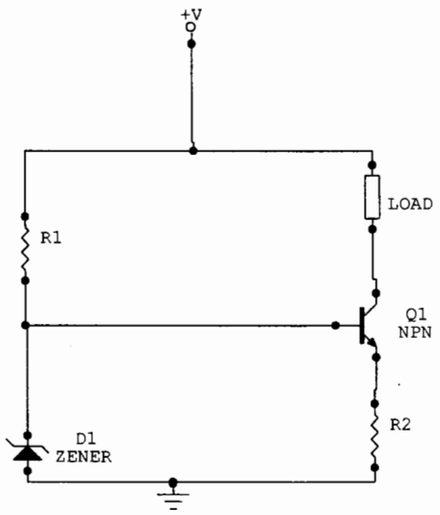

Figure Q4.A

B) Draw the circuit diagram of a basic BJT current mirror. Derive an exact equation relating the two currents being mirrored. What is the effect of the Early Voltage on the expression you have derived? **6** marks

C) For a Darlington Emitter follower circuit, determine the input resistance, the current gain and the voltage gain of the overall circuit. The transistors used are identical with parameters: R_e = 4 kΩ, h_{fe} =50, h_{ie} = 1100 kΩ, h_{oe} = 24 μA/V. **8** marks

Q 5

A) An amplifier is given with a voltage gain of A_v = 10. An engineer manages, with suitable feedback connection to raise the voltage gain to A_v =100. Is the connection used a positive or a negative feedback? How much is the loop gain of this connection? Explain your answer. **3** marks

B) An opamp has the following parameters: A_{vOL} = 2x105, r_{in} = 2 MΩ and r_o = 75 Ω. Design an inverting voltage amplifier with an input resistance of at least 1 kΩ and output resistance of less than 0.01 Ω. You may make any reasonable assumptions in your design.

What would be the largest gain obtainable with these specifications? Justify your answer. **9** marks

C) For the circuit shown Fig. 5C, calculate A_{VF}, R_{OF}, and R_{IF}, assume Rs= 0, h_{fe} =50, h_{ie} = 1.1 K, h_{re}= h_{oe} = 0, and identical transistors. **8** marks

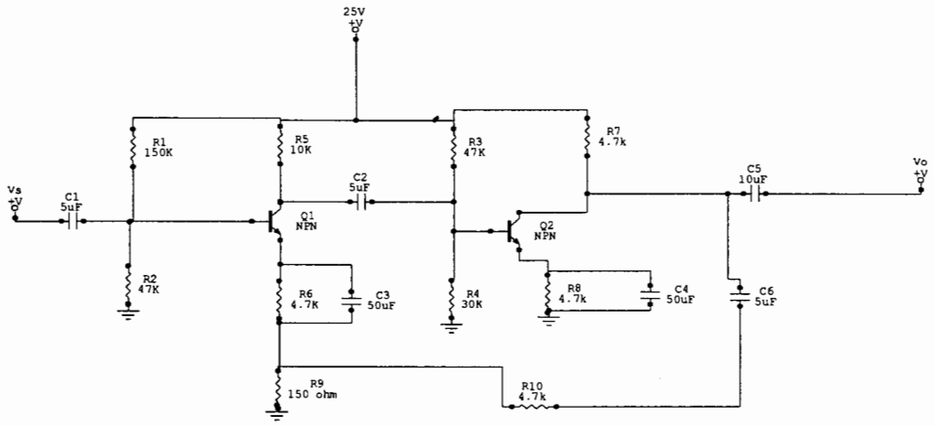

Figure Q.5C Second collector to first emitter feed back pair.

Q 6

A) Why CMOS technology is preferred to design ICs? **2** marks

B) What are the steps involved in fabricating a monolithic integrated circuit, explain briefly with neat diagrams. ***10*** marks

C) Mention different types of CCDs and how charges can be stored and transferred between potential wells? Explain with suitable diagrams

8 marks