UNVERSITY OF SWAZILAND

MAIN EXAMINATION – SEMESTER II MAY 2011

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF THE PAPER: ANALOG ELECTRONICS IV

COURSE CODE: E512

TIME ALLOWED: 3 HOURS

INSTRUCTIONS:

1. **Answer any FOUR (4) of the six questions. Each question carries 25 marks.**
2. **If you think not enough data has been given in any question you may assume any reasonable values.**
3. **A sheet with useful RF design formulae is attached at the end of the paper.**
4. **Impedance-Admittance (Z-Y) Smith Charts are provided.**

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS NINE (9) PAGES INCLUDING THIS PAGE.

QUESTION ONE ***(25 Marks)***

(a) (i) What are the requirements of a good quality audio power amplifier output stage? *(2 marks)*

(ii) Does a common-emitter stage meet the requirements you have mentioned in (i)? Briefly discuss your answer. *(3 marks)*

(b) A power BJT is specified to have $T_{Jmax} = 175°C$ and $P_{Dmax} = 130$ W for $T_C \leq 25°C$. For $T_C \geq 25°C$, $\theta_{JC} = 1.2$ °C/W. The device is required to dissipate 60 W while operating at an ambient temperature of 25°C.

(i) Find the thermal resistance of a suitable heatsink that must be used assuming that $\theta_{CS} = 0.5$ °C/W. *(4 marks)*

(ii) Determine the case temperature of the BJT. *(2 marks)*

(c) Consider the emitter follower output stage shown in Fig. Q.1c.

(i) Explain why there are two limits for the negative swing of the output voltage. *(4 marks)*

(ii) With a sinusoidal input signal the circuit is required to deliver 2W into a 100-Ω load resistance R_L. Design the circuit specifying appropriate supply voltages and resistor R. You may neglect transistor saturation voltages in your design. *(6 marks)*

(iii) Calculate the power conversion efficiency of the circuit designed in (ii) when delivering its rated output power. *(4 marks)*

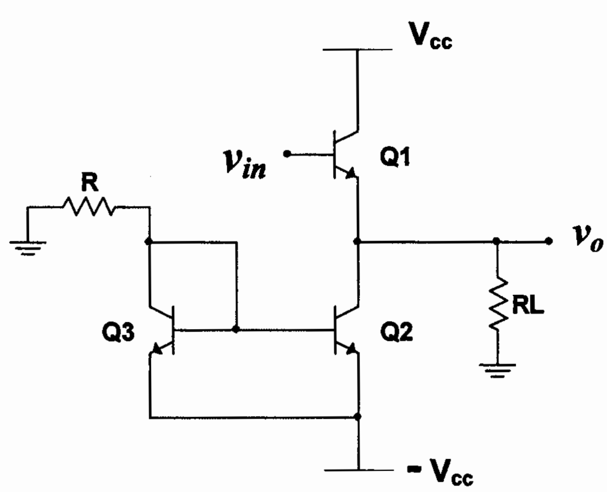


Fig. Q.1c

QUESTION TWO ***(25 Marks)***

A circuit of a Class AB amplifier output stage is shown in Fig. Q.2. Assume that transistors Q_1 and Q_2 are matched, as are Q_3 and Q_4.

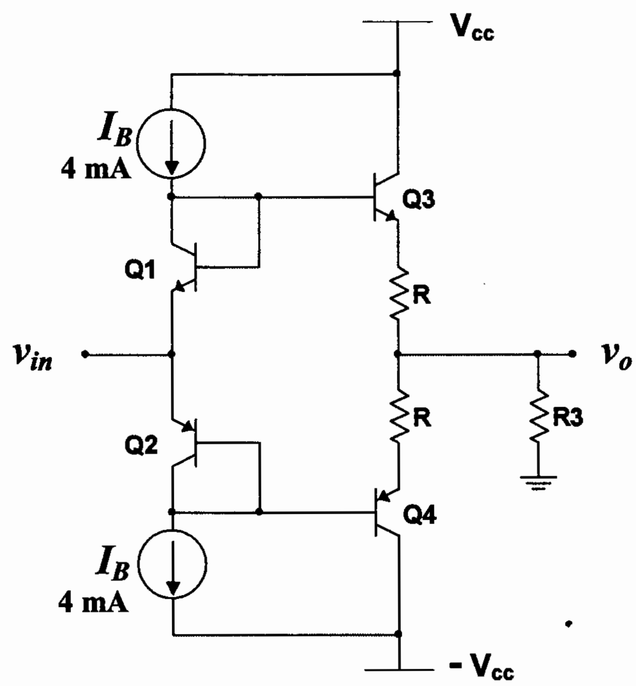


Fig. Q.2

(a) Explain the purpose of transistors Q_1 and Q_2. *(2 marks)*

(b) Using the basic large-signal equation, $I_c = I_s e^{v_{BE}/v_T}$, consider the upper half of the circuit and neglect the base currents. Show that at quiescent conditions (i.e $v_{in} = 0$) the currents I_B and I_{c3} are related by

$$I_B = \left(\frac{I_{s1}}{I_{s3}}\right) I_{c3} e^{(I_{c3}R)/v_T}$$

Hint: When $v_{in} = 0$, $v_o = 0$. Why is this so? *(6 marks)*

(c) If $I_{s1} = 0.3$ pA and $I_{s3} = 4.5$ pA find the value of resistor R required to give a quiescent current of 5 mA in the output transistors. *(4 marks)*

(d) When the output stage is delivering 150 mA into the load and $\beta = 100$ for all transistors:

(i) Calculate the base–emitter voltage of Q_3 assuming that Q_4 is carrying negligible current. *(4 marks)*

(ii) Calculate also the emitter voltages of Q_1, Q_2 and Q_4. *(5 marks)*

(iii) Hence show that the assumption in (i) is valid. *(4 marks)*

QUESTION THREE ***(25 Marks)***

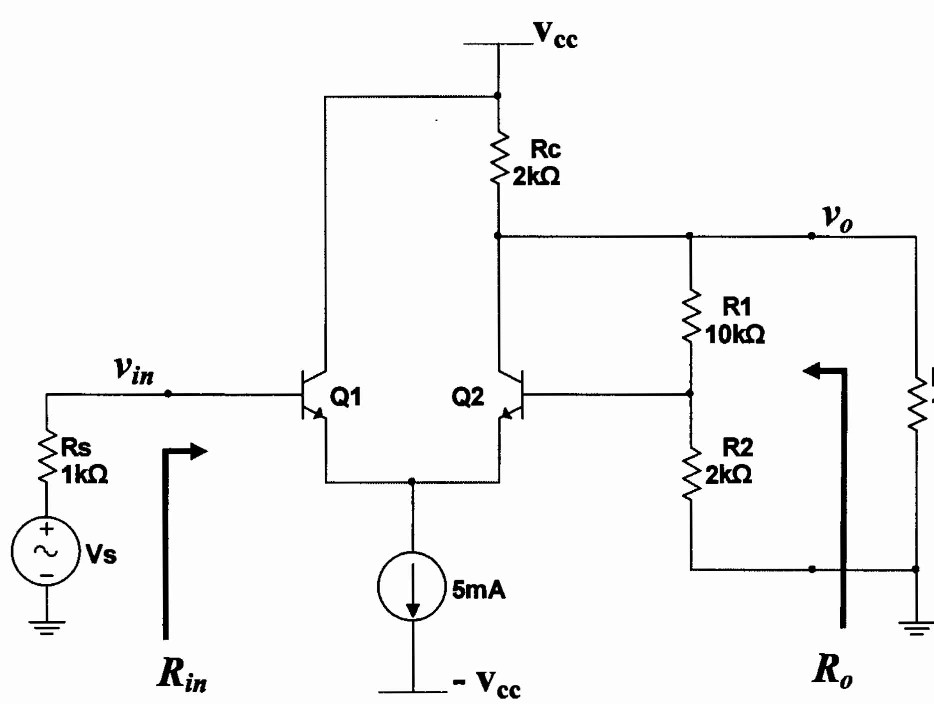
(a) A 741 opamp is specified as follows: $A_v = 200{,}000$ V/V, $r_{in} = 2$ MΩ, $r_{out} = 75\,\Omega$. It is desired to use the 741 in a feedback configuration to obtain an amplifier with input resistance of **at least** 1000 MΩ and an output resistance of **less than** 0.1 Ω.

(i) Which feedback configuration should be used in the required amplifier? Explain your answer. *(3 marks)*

(ii) What is the largest gain achievable in the amplifier which meets the specifications? *(5 marks)*

(iii) Design the amplifier giving components value for the feedback network. *(4 marks)*

(b) For the amplifier shown in Fig. Q.3b, assume that the transistors Q1 and Q2 are matched with $\beta = 100$. Use feedback principles to obtain the voltage amplification factor $\frac{v_o}{v_{in}}$ input impedance R_{in} and output impedance R_o. *(13 marks)*



QUESTION FOUR ***(25 Marks)***

(a) Manufacturer's noise data for the 2N5210 npn BJT are shown in Figs. Q4a.1 and Q4a.2. on the next page. The device is to be used at 200 Hz with a source resistance of 500 Ω and a collector bias current of 3 mA. Assume room temperature operation at $T = 293$ K.

(i) Calculate its total equivalent input noise per $\sqrt{\text{Hz}}$. *(10 marks)*

(ii) Calculate the narrow bandwidth Noise Figure. *(4 marks)*

(b) A dc blocking L-section matches a 300 Ω load to a 50 Ω transmission line, the operating frequency being 500 MHz. Using the Q-method, determine the component values of the matching network. *(11 marks)*

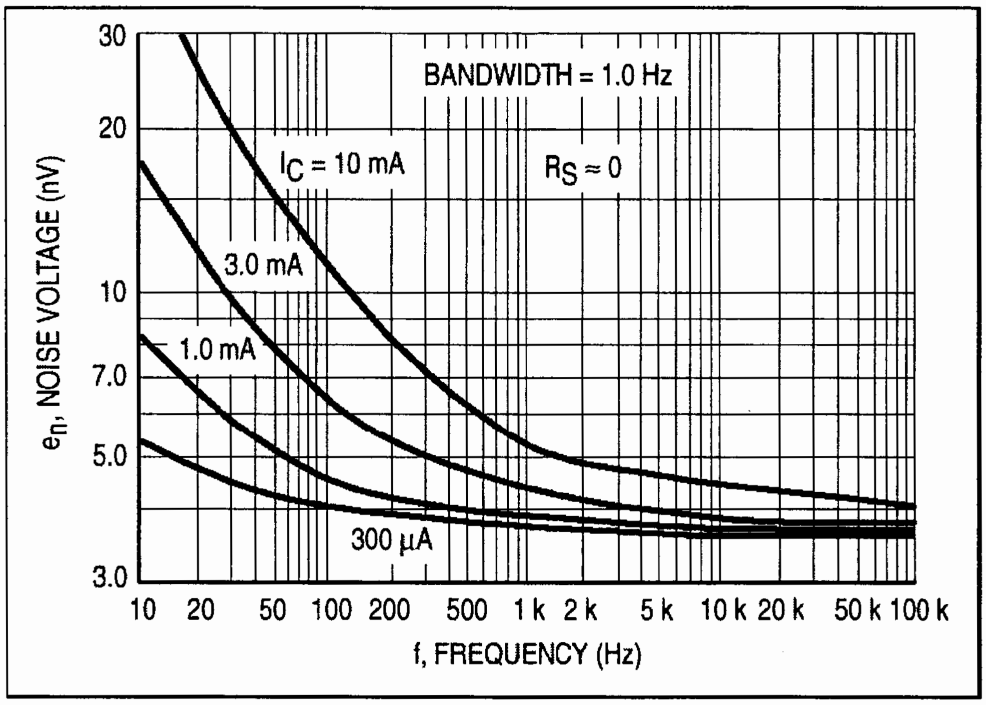


Fig. Q4a.1 Motorola 2N5210 npn BJT: Noise voltage vs. frequency, for various quiescent collector currents, with Rs=0 and BW = 1 Hz.

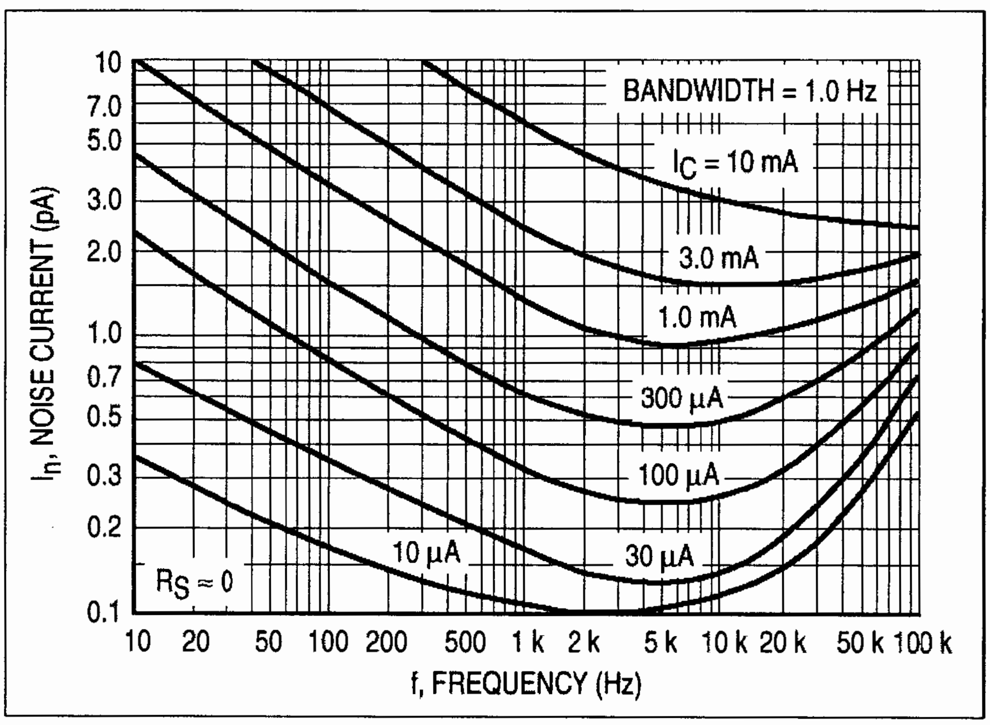


Fig.Q 4a.2 Motorola 2N5210 noise current vs. frequency, for various quiescent collector currents.

QUESTION FIVE *(25 Marks)*

An RF transistor biased at $V_{CE} = 10$ V and $I_C = 5$ mA has the following S=Parameters at 1 GHz. The parameters are based on 50-Ω terminations.

$$S_{11} = 0.68\angle 178^{o} \qquad S_{21} = 6.6\angle 77^{o}$$

$$S_{12} = 0.03\angle 53^{o} \qquad S_{22} = 0.46\angle -32^{o}$$

(a) Is this transistor stable with a source impedance of 300 Ω and a load of 30 Ω at this frequency? Justify your answer. *(8 marks)*

(b) What is the Maximum Available Gain of this transistor? Under what condition is this obtained? *(8marks)*

(c) If the source impedance is 300 Ω and the load impedance is 30 Ω and S_{12} is assumed to be negligibly small, show with a circuit sketch how maximum gain can be obtained. Components values are not required, but you should indicate whether the components in your circuit are inductors or capacitors. *(9 marks)*

QUESTION SIX ***(25 Marks)***

(a) A source of 1.2 GHz is matched to a load by a matching network consisting of a transmission line and a shunt capacitor C as shown in Fig, Q6a. If the characteristic impedance of the transmission line is 50 Ω, find the required length of the line and the required value of the capacitance C using the Z-Y Smith Chart. Assume that the velocity of propagation in the transmission line is 2.2×10^8 m/s. *(19 marks)*

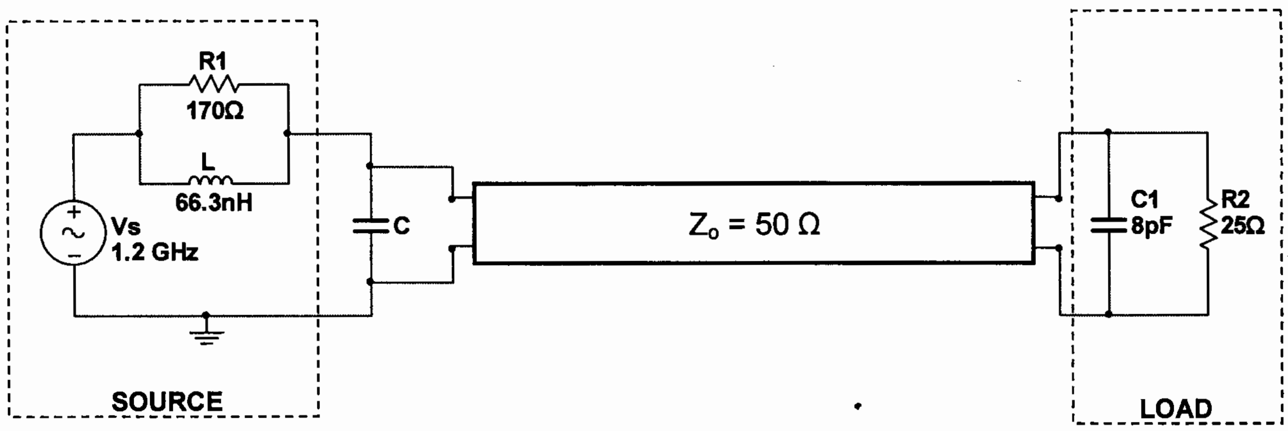


Fig Q6a

(b) Design a dc passing L network to match a 100-Ω source to a 10-Ω load at a frequency of 1 GHz. *(6 marks)*

SOME SELECTED USEFUL RF DESIGN FORMULAE

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|^2}$$

$$\text{where } |\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$$

$$\text{MAG} = 10\log\left|\frac{S_{21}}{S_{12}}\right| + 10\log\left|K - \text{sgn}(B_1)\sqrt{K^2 - 1}\right| \quad \text{dB}$$

$$\text{where } B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$