UNIVERSITY OF SWAZILAND

SUPPLEMENTARY EXAMINATION, JULY 2011

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE ELECTRONICS IV
COURSE CODE:	E512
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. A sheet with useful RF design formulae is attached at the end of the paper.
4. Impedance-Admittance (Z-Y) Smith Charts are provided.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

(a) An output stage of an amplifier is shown in Figure-Q1.

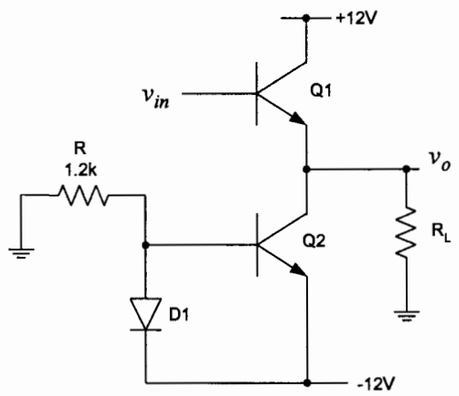

Figure-Q1

(i) Identify the type of the amplifier stage shown and sketch the transfer characteristic(v_o vs v_{in}). **(3 marks)**

(ii) If the ratio of emitter junction area of Q_2 to the junction area of D_1 is 50 $\left(i.e\ \frac{A_{jQ2}}{A_{jD1}} = 50\right)$, find the value of R_L for which the output signal is maximum. You may neglect the base currents and the saturation voltages. **(5 marks)**

(iii) Calculate the maximum output power and the power conversion efficiency. **(5 marks)**

(b) (i) Draw the safe operating area (SOA) of a BJT and identify the limits of operation. **(3 marks)**

(ii) Some values referred from a BJT data sheet are given below.

$T_{j\max} = 150^0 C$ $\qquad P_{D\max} = 2.5W\ \left(at\ T_A = 25^0 C\right)$

$P_{D\max} = 50W\ \left(at\ T_C = 25^0 C\right)$

Find the maximum power dissipation this device can handle in free air when it is used in an ambient temperature of $40^0 C$. If this device is required to dissipate 30W at the ambient temperature of $40^0 C$, find the specification of the required heat sink. Also calculate the temperature of the heat sink at the steady state. Assume $\theta_{CS} = 0.5\ ^0 C/W$.

(9 marks)

QUESTION TWO *(25 marks)*

Consider the class AB amplifier output stage in Figure-Q2. The transistors are of silicon and Q_2, Q_3 are matched.

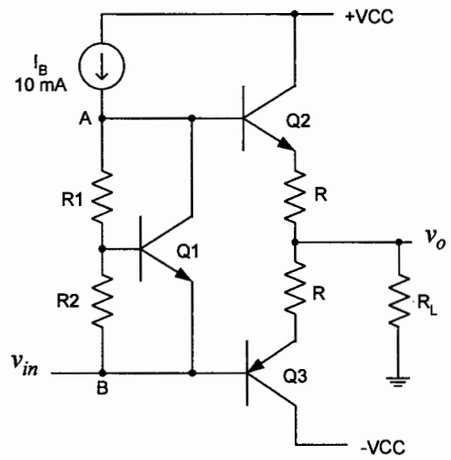

Figure-Q2

(a) Explain the function of Q1. **(4 marks)**

(b) If $R = 0$ and under quiescent conditions (*i.e* $v_{in} = 0$), show that

$$I_{C2} = I_{S2}\left(\frac{I_B}{I_{S1}}\right)^{\frac{1+K}{2}} \quad \text{where} \quad K = \frac{R_1}{R_2}.$$

You may use the large signal equation $I_C = I_S e^{\frac{V_{BE}}{V_T}}$. Neglect the base currents and the currents in R_1 and R_2. **(8 marks)**

(c) When $R = 2.2k$, $I_{S1} = 0.4pA$ and $I_{S2} = 6pA$, find the value of K to have a quiescent current of $10mA$ in the output transistors. **(6 marks)**

(d) Find V_{AB} when the current in Q_2 is $300mA$ and compare it with its value under the quiescent conditions. Assume for Q_2 and Q_3, the current gain $\beta = 100$ and for Q_1 the gain is high. The value of K is same as in (c). **(7 marks)**

QUESTION THREE *(25 marks)*

A load of 120Ω is matched to a 50Ω source using a transmission line and an inductor as shown in Figure-1.

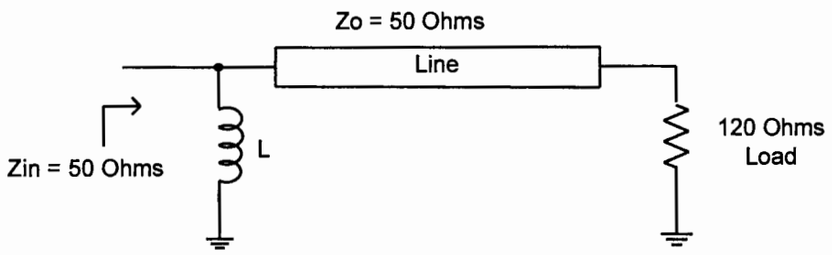

Figure -1

Using the ZY Smith Chart find the length of the transmission line and the value of inductance L at 10 MHz. Assume that the speed of propagation in the transmission line is 2.2×10^8 m/s.

(25 marks)

QUESTION FOUR (*25 marks*)

(a) If the parallel combination of resistor R_P and reactance jX_P is transformed to the series combination of resistance R_S and reactance jX_S, show that the Q of the combinations is given by

$$Q = \sqrt{\left(\frac{R_P}{R_S} - 1\right)}$$

(5 marks)

(b) Design a dc passing L network to match a load of 600Ω to a source of 50Ω at 200MHz.
(10 marks)

(c) If the noise generated in an amplifier is represented by the two input noise generators of instantaneous noise voltage e_n and instantaneous noise current i_n, show that the optimum source resistance for minimum noise factor is given by

$$R_{S(opt)} = \left(\frac{\overline{e_n^2}}{\overline{i_n^2}}\right)^{\frac{1}{2}}.$$

(10 marks)

QUESTION FIVE (25 *marks*)

The s-parameters of a transistor used in a common emitter amplifier at 1 GHz and operating with $V_{CE} = 15V$, $I_C = 5mA$ are given below.

$$S_{11} = 0.68 \angle 178^0 \quad S_{21} = 6.6 \angle 77^0 \quad S_{12} = 0.03 \angle 53^0 \quad S_{22} = 0.46 \angle -32^0$$

(a) Investigate the stability of the amplifier using this transistor at 1 GHz with source and load impedance of 50Ω. **(10 marks)**

(b) Evaluate the maximum available gain. **(7 marks)**

(c) Assuming $S_{12} = 0$, give the schematic diagram of a maximum gain amplifier indicating the type of the components. You need not to give the values of the components. **(8 marks)**

SOME SELECTED USEFUL RF DESIGN FORMULAE

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|^2}$$

$$\text{where } |\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$$

$$\text{MAG} = 10\log\left|\frac{S_{21}}{S_{12}}\right| + 10\log\left|K - \text{sgn}(B_1)\sqrt{K^2 - 1}\right| \quad \text{dB}$$

$$\text{where } B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$