UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

MAIN EXAMINATION	2010/2011
TITLE OF PAPER:	BASIC ELECTRONICS
COURSE NUMBER:	EE221
TIME ALLOWED:	3 HOURS

INSTRUCTIONS:

ANSWER ANY FOUR OUT OF FIVE QUESTIONS.

EACH QUESTION CARRIES 25 MARKS.

MARKS FOR DIFFERENT SECTIONS ARE SHOWN ENCLOSED IN SQUARE BRAKETS.

THIS PAPER HAS 5 PAGES INCLUDING THIS PAGE.

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1. (a) The simple voltage regulator circuit shown in Fig. 1 of the appendix uses a 6.3 volts Zener diode with a maximum power rating of 300 mW. It is required to hold the voltage across the load substantially constant as the circuit input voltage varies between 10 V and 20 V. Calculate a suitable range of values for the series resistance, R_s to ensure that the Zener diode operates below it's maximum power rating. **[8]**

(b) A half-wave rectifier operating from a 50 Hz supply provides a peak output of 30 V. A load resistance of 20 kΩ is put across the output with a reservoir capacitor in parallel. Calculate the capacitance of the capacitor required if the ripple voltage is to have a peak value of 2 V. **[9]**

(c) An applied AC voltage is given by, $v = v_0 e^{j\omega t}$ where the complex number, $j = e^{j\frac{\pi}{2}}$:

(i) Show that in an AC circuit containing pure inductance the current lags behind the applied voltage by $\pi/2$; **[4]**

(ii) Show that in an AC circuit containing pure capacitance the current leads the applied voltage by $\pi/2$. **[4]**

2. (a) Determine the transfer function of a first order low-pass *RC* filter. **[7]**

(b) Show that the power output is half of the input for a low-pass filter at the cut-off frequency. **[6]**

(c) A first- order *RC* low-pass filter is to be designed to give a cut-off frequency of 0.5 kHz.

(i) What capacitance would be required if the resistance, *R* is 0.5 kΩ? **[4]**

(ii) By how much would the output voltage of the filter be attenuated at the cut-off frequency (in decibels)? **[4]**

(iii) What would be the phase difference between the output and input voltages at the cut-off frequency? **[4]**

3. (a) State Thevenin's theorem as applied to a two-terminal network of resistors and sources of emf. **[3]**

(b) In the BJT amplifier in Fig. 2 of the appendix, the value of β for the transistor is 100 and V_{BE} is 0.7 V.

(i) Determine the DC Thevenin equivalent circuit for the input bias. **[3]**

(ii) Determine the DC operating point currents, I_B, I_C and I_E. **[3]**

(iii) Determine the DC operating point voltages, V_C, V_E and V_B. Hence show that the npn transistor is forward active. **[4]**

(iv) Convert to an AC-only model and Thevenize the entire circuit. Assume that the

capacitors C_1, C_2 and C_3 are large. **[4]**

(v) Replace the transistor with a small signal model and re-draw the circuit. **[2]**

(vi) Calculate the gain of the amplifier given that the transconductance $g_m \approx 40I_C$, the transistor input resistance is $r_\pi = \frac{\beta}{g_m}$ and it's output resistance $r_o = 45.2\ \text{k}\Omega$. **[6]**

4. (a) (i) Sketch the circuit diagram of a logarithmic amplifier which utilizes a pn junction diode. **[2]**

(ii) Show that the output voltage, v_o of a logarithmic amplifier is related to the input voltage, v_i by:

$$v_o = -2.303\eta V_T \log_{10}\left(\frac{v_i}{I_0 R}\right)$$

where the symbols have their usual meaning. **[6]**

(b) Derive the general feedback equation for an amplifier. **[4]**

(c) A voltage amplifier has an open-loop gain of -800. If 0.5% of the output voltage is fed back to the input as negative feedback, what will be the percentage change in the gain with feedback when the open-loop gain decreases by 10%, due to changes in device parameters? **[9]**

(d) A resistor, R and capacitor, C are used the form an op-amp differentiator that gives an output of -5 V for an input rate of change of +10 V/s. The same resistor and capacitor are then used to form an op-amp integrator. Find the expression for the output of the integrator in terms of it's input. **[4]**

5. (a) What logic function, F does the circuit in Fig. 3 of the appendix represent? **[6]**

(b) Reduce the following Boolean functional expression to only two terms:

$$F = A\overline{(A\bar{B} + \bar{A}B)}.$$ **[7]**

(c) Draw a Karnaugh Map in three variables A, B and C for the expression F given as:

$$F = C + A\bar{B}.$$ **[4]**

(d) Use a Karnaugh map to minimize the logic expression for the operation specified by the truth table in Table 1 of the appendix and design a logic circuit to implement it. **[8]**

APPENDIX – DIAGRAMS

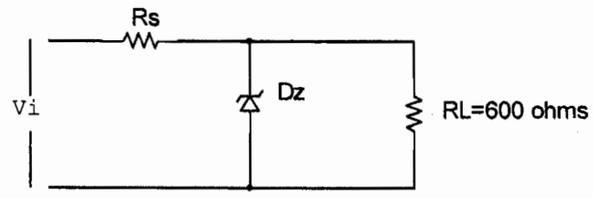

Figure 1

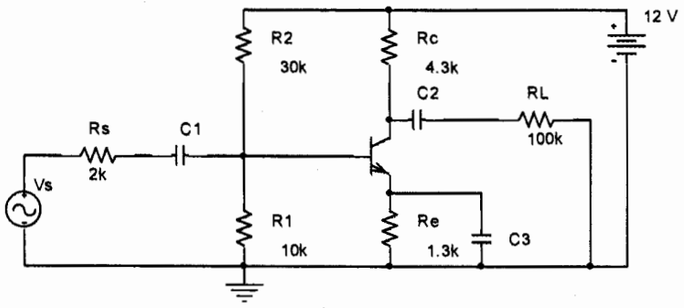

Figure 2

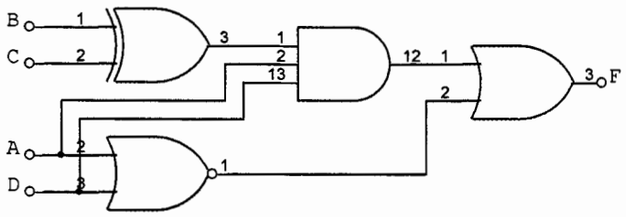

Figure 3

INPUTS			OUTPUTS
A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Table 1

END OF EE221 EXAMINATION