UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

DIGITAL SYSTEMS I

COURSE CODE – EE322

MAIN EXAMINATION DECEMBER 2010

DURATION OF THE EXAMINATION - 3 HOURS

INSTRUCTIONS TO CANDIDATES

i. There are FIVE questions in this paper. Answer any FOUR questions only.

ii. Each question carries equal marks.

iii. Show all your steps clearly in any calculations.

iv. State clearly any assumptions made.

v. Start each new question on a fresh page.

DO NOT OPEN THIS PAPER UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

Question 1

(a) Using the tabular method, minimize the following Boolean function:

$$F(A, B, C, D) = \sum (1, 3, 4, 5, 10, 11, 12, 13, 14, 15) \quad [8]$$

(b) Simplify the following using a k-map:

(i) $F = wxy + yz + x'z + x'y$ [7]

(ii) $F(A, B, C, D) = \sum(1, 3, 5, 7, 9, 15)$ [4]
$d(A, B, C, D) = \sum(4, 6, 12, 13)$

(c) Using Boolean algebra simplify the following expressing to a minimum number of literals:

$$F = (x'y' + z)' + z + xy + wz \quad [6]$$

Question 2

(a) Consider the combinational circuit shown in Figure Q2.

(i) Derive the Boolean Expressions for F0 and F1 [4]
(ii) Determine the truth table of the circuit. [8]
(iii) Minimize the circuit and show that simplified Boolean expressions are equivalent to the ones obtained in (i). [9]

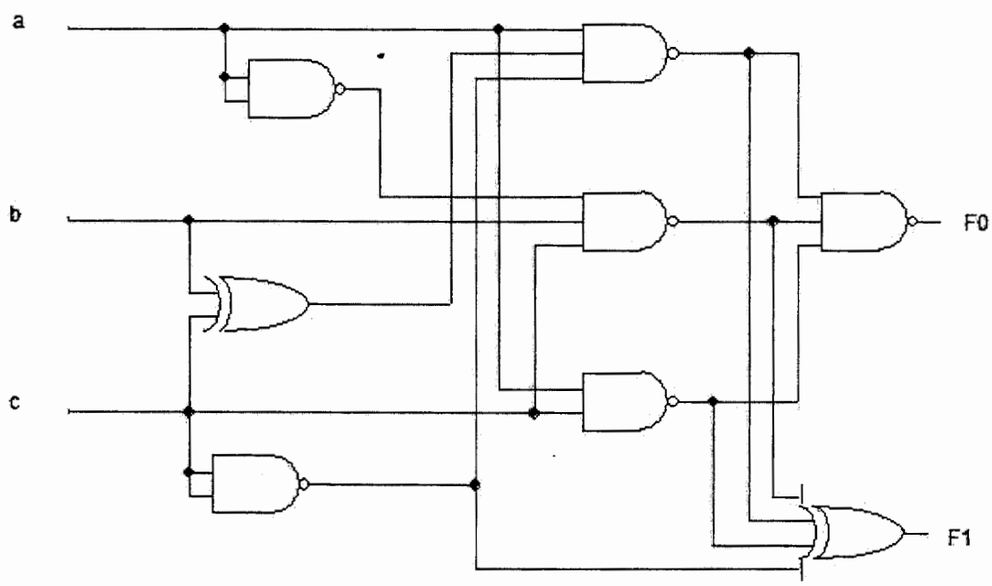

Figure Q2: Diagram for question 2 (a)

(b) Prove that the XOR is an odd function for any number of bits n. [4]

Question 3

a) A combinational circuit is defined by the following three Boolean functions:

$$F_1 = x'y'z' + xz$$
$$F_2 = xy'z' + x'y$$
$$F_3 = x'y'z + xy$$

Design the circuit with a decoder and external gates. [7]

b) Specify the truth table of an octal-to-binary priority encoder. Provide an output V to indicate that at least one of the inputs is present. The input with the highest subscript number has the highest priority. What will be the value of the four outputs if inputs D5 and D3 are at 1 at the same time? [7]

c) Implement a full adder with two multiplexers. [6]

d) An 8 x 1 multiplexer has inputs A, B, and C connected to the selection inputs S_2, S_1, and S_0, respectively. The data inputs I_0 through I_7 are as follows: $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$; and $I_6 = D'$. Determine the Boolean function that the multiplexer implements (express it is sum of products). [5]

Question 4

a) Derive the Boolean expressions for the output sum and output carry in a full adder circuit with inputs x_i, y_i, and c_i. [6]

b) Define the carry propagate and carry generate as

$$P_i = x_i + y_i$$
$$G_i = x_i y_i$$

respectively. Show that the output carry and output sum of a full adder becomes

$$C_{i+1} = (C'_i G'_i + P'_i)' \quad [8]$$
$$S_i = (P_i G'_i) \oplus C_i \quad [7]$$

c) Design a half-subtractor circuit with inputs x and y and outputs D and B. The circuit subtracts the bits x – y and places the difference in D and the borrow in B. [4]

Question 5

a) Define the following terms as used in digital electronics:
   i. Combinational circuit
   ii. Sequential circuit
   iii. Magnitude Comparator

[6]

b) Design a 4-bit Magnitude Comparator which compares two 4-bit binary numbers A, B and determines whether A<B, A>B, or A=B.

[12]

c) Implement the following function using NAND gates only:

$$F(x,y) = (x \oplus y)(x+y)'$$

[7]

END OF PAPER