UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

DIGITAL SYSTEMS II

COURSE CODE – EE324

MAIN EXAMINATION MAY 2011

DURATION OF THE EXAMINATION - 3 HOURS

INSTRUCTIONS TO CANDIDATES

1. There are FIVE questions in this paper. Answer any FOUR questions only.
2. Each question carries equal marks.
3. Show all your steps clearly in any calculations.
4. State clearly any assumptions made.
5. Start each new question on a fresh page.

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Question 1

Derive the state table, state diagram, and Boolean expressions for the outputs O0 to O2 in the circuit diagram shown in Figure Q1. **[25]**

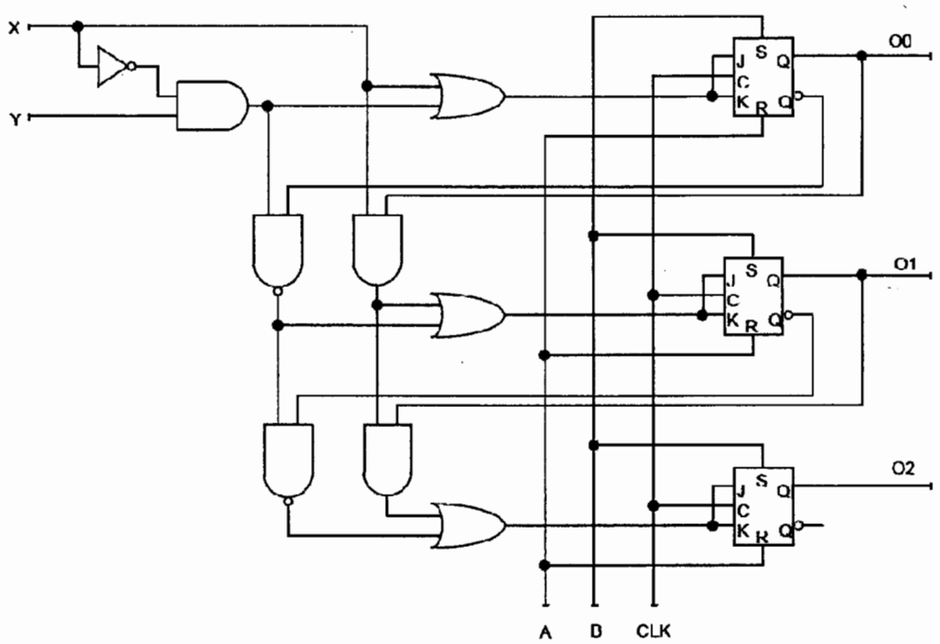

Figure Q1. Circuit diagram for Question 1

Question 2

Using T Flip-Flops, design a Mealy sequential circuit that detects the sequence 1010. Use a minimum number of states and external gates in your implementation. [25]

Question 3

Design a versatile 4-bit shift register capable of operating in the following modes:

(i) converting data from parallel to serial

(ii) converting data from serial to parallel

(iii) parallel input and output of data

(iv) shifting data from left to right and from right to left

Explain in detail how your design meets the above requirements. [25]

Question 4

(i) With the aid of a diagram (or diagrams), explain how a Master-Slave D flip-flop works. Explain the rationale for having this type of circuit edge-triggered rather than level-triggered.

[5]

(ii) Design a timing circuit that provides an output signal that stays on for exactly eight clock cycles. A start signal sends the output to the 1 state, and after eight clock signals returns to the 0 state.

[14]

(iii) Discuss the instruction execution cycle in a microprocessor. [6]

Question 5

Figure Q5 shows a two lane busy road that passes over a narrow bridge. Due to the narrow bridge, traffic coming from opposite directions (Traffic A and B) cannot pass over the bridge at the same time. To ensure an orderly flow of traffic over the bridge, the traffic control lights have been introduced. Each traffic light has a RED, AMBER, and GREEN lamps.

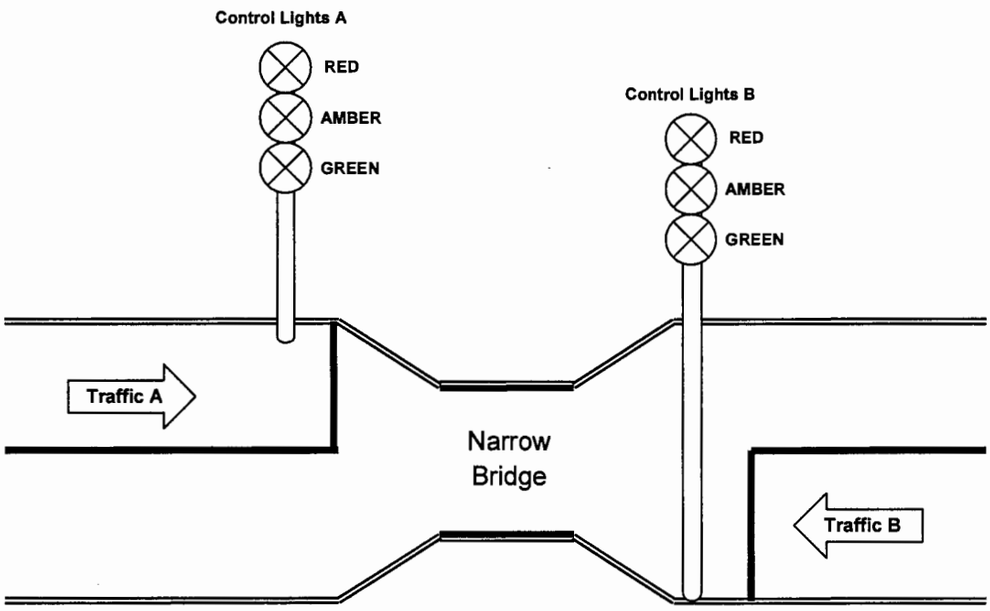

Figure Q5. Traffic control lights diagram for Question 5

The traffic control lights are required to operate so that traffic flows as follows: Traffic B is allowed 1 minute to pass through, while traffic A is allowed 2 minutes. Traffic A is allowed to pass through the bridge when the GREEN light in Control Lights A is ON, otherwise the Traffic A is stopped. Similarly traffic B can only pass through the bridge when the GREEN lamp in traffic control B is on. When a traffic control light turns from GREEN to RED, for 3 seconds, it turns ON the AMBER light and then switch on

the RED lamp. Assume that, initially (before the control regime come into effect), all traffic is stopped for 10 seconds.

Design a traffic controller that ensures an orderly flow of traffic in Road 1, Lane A, and Lane B, using a suitable counter(s) and a ROM to satisfy the requirements of the traffic control regime. Assume that a clock frequency of 1Hz is used for driving the counter. Show all working and explain how your circuit works.

[25]

END OF PAPER